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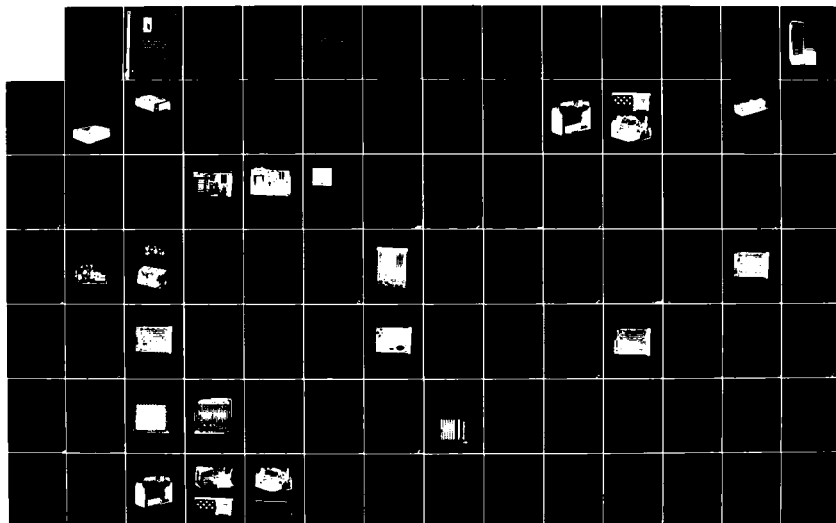
MULTIMODE GUIDANCE PROJECT LOW FREQUENCY ECM SIMULATOR:
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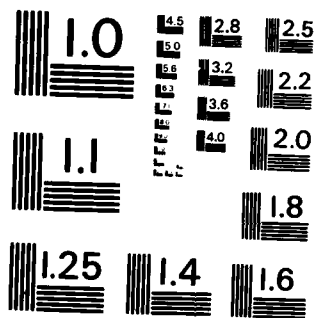
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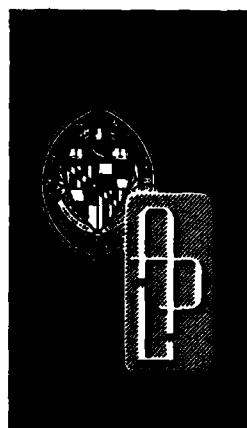
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Technical Memorandum

**MULTIMODE GUIDANCE PROJECT
LOW FREQUENCY ECM SIMULATOR:
HARDWARE DESCRIPTION**

H. M. KAYE

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Johns Hopkins Road, Laurel, Maryland 20707
Operating under Contract N00024-83-C-5301 with the Department of the Navy

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ABSTRACT

The Multimode Guidance (MMG) Project, part of the Army-Navy Area Defense SAM Technology Prototyping Program, was established to conduct a feasibility demonstration of multimode guidance concepts. Prototype guidance units for advanced, long range missiles are being built and tested under MMG Project sponsorship.

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1. INTRODUCTION

The Multimode Guidance (MMG) Project, part of the Army/Navy Area Defense SAM Technology prototyping Program, was established to conduct a feasibility demonstration of multimode guidance concepts. Prototype guidance units for advanced, long range missiles are being built and tested under MMG Project sponsorship.

The Johns Hopkins University Applied Physics Laboratory has been designated as Government Agent for Countermeasures for this project. In support of this effort, a family of computer-controlled ECM simulators is being developed for validation of contractor's multimode guidance prototype designs.

The development of a Low Frequency ECM Simulator has been completed. This computer-controlled simulator can simulate up to six surveillance radar jammers in B through F bands and will be used to

evaluate the performance of home-on-jamming guidance modes in multiple jammer environments. This system provides a unique capability in that a test operator can program a desired ECM test scenario with either fixed or time-varying parameters. The flexibility and repeatability of programmable computer control of six independent RF sources makes the MMG Low Frequency ECM Simulator an extremely powerful and versatile ECM test simulator.

The design of the Low Frequency ECM Simulator is documented in two volumes; Volume A describes the hardware design of the simulator and Volume B describes the software design. This document, Volume A, describes the Low Frequency ECM Simulator system hardware design in two levels of detail. The main body of the report provides functional descriptions to the block diagram level; the appendixes provide specific detailed circuit descriptions and associated schematic drawings.

2. MAJOR PERFORMANCE CHARACTERISTICS

The major performance characteristics of the MMG Low Frequency ECM Simulator are listed below:

1. Six independent RF channels:
Three channels (type I), 250 MHz to 1 GHz
Three channels (type II), 1 to 4 GHz
2. RF power output: type I, +20 dBm; type II, +17 dBm
3. RF resolution: 1 to 8 MHz, (minimum resolution step = $1/256$ of VCO bandwidth)
4. ECM noise types: spot, barrage, pulsed, swept, Gaussian, non-Gaussian, and combinations
5. FM modulation sources: Gaussian noise, multiprogrammer D/A, Wavetek 175, external
6. Noise video bandwidth: 1 kHz, 10 kHz, 100 kHz, 1 MHz, and 5 MHz
7. Noise RF bandwidth: up to 40% of RF band
8. Noise fill oscillator: 100 KHz
9. AM modulation sources: multiprogrammer D/A, Wavetek 175, external
10. AM modulator range: 55 dB, linear
11. Pulse modulation sources: 10 and 100 Hz internal oscillator, multiprogrammer timer/pacer card, Wavetek 175, external
12. Biphase modulators: 5, 10, and 20 MHz comb; 10, 20, and 40 MHz pseudorandom code, or external
13. Level-set attenuators: 81 dB range in 1 dB steps

3. SYSTEM FUNCTIONAL DESCRIPTION

General

The MMG Low Frequency ECM Simulator has the following principal features:

1. Full software control of ECM simulator output,
2. Multiple frequency band coverage with multiple sources in each band,
3. Independently produced modulation formats, which can be combined as required,
4. Simultaneous amplitude, frequency, pulse, and biphase modulations of each RF source,
5. Formation of arbitrary waveforms,
6. Coordination of RF channel outputs,
7. Control via standard IEEE-488 data bus.

Figure 1 is a photograph of the MMG Low Frequency ECM Simulator and the HP 9825S computer/controller. Six fully independent RF channels are shown, mounted in the upper portion of the ECM simulator rack, while the lower portion contains two Wavetek 175 arbitrary waveform generators and a HP 6942/6943 multiprogrammer/extender. Each RF channel contains two single-octave bandwidth VCO modules, (one of which is available at a time) to permit frequency coverage of two octaves. The type I channels cover 250 MHz to 1 GHz and the type II channels, 1 to 4 GHz. Three channels of each type are included in the system. The system is controlled by an HP 9825S computer over an IEEE-488 standard bus interface.

The HP 6942/6943 multiprogrammer/extender acts as a control interface between the computer and the six RF channels. Digital output cards in the HP 6942/6943 are used for frequency tuning and channel control functions. Digital-to-analog converter cards provide programmable AM and FM modulation sources, and a pulse generator card provides a programmable pulse modulation source. The multiprogrammer also acts as a control interface for the level-set attenuator driver and for the AM and FM switch matrixes.

The two arbitrary waveform generators (Wavetek 175) provide additional sources of AM, FM, and pulse modulation. They can be programmed to generate sinusoidal, square-wave, triangular, and ramp waveforms as well as any arbitrary waveform that can be specified by amplitude as a function of time.

These outputs are connected to the appropriate RF channels by AM and FM switching matrixes. A block diagram of the system, including a detailed block diagram of one of the six RF channels, is shown in Fig. 2.

The fundamental modulation format for an RF channel is frequency modulation of the VCO. FM modulating signals may be obtained from a Gaussian noise source, a fill oscillator, or an auxiliary channel that can be driven by either of the Wavetek 175 generators or by an external function generator. These modulation sources may be combined as desired under computer control to produce RF spot bandwidths ranging from less than 1 MHz to about 40% of the VCO bandwidth.

An operator may also program linear amplitude modulation of the VCO signal with a range of 0 to 55 dB from one of three sources. The source of the modulating AM signal may be either a D/A converter card, the Wavetek 175, or an external function generator.

Biphase modulation is available to produce either comb or pseudorandom noise spectra. Three internal clock frequencies are available along with provision for an external input to generate noise of up to 40 MHz bandwidth or combs with up to 20 MHz tooth spacings.

An operator may also blink or pulse modulate the RF signal. Five programmable sources internal to the ECM simulator or an external source may be used to generate pulse trains with a maximum PRF of 500 kHz and a variable duty cycle.

The RF power output of the system is +20 dBm in the 250 MHz to 1 GHz range and +17 dBm in the 1 to 4 GHz range. A level-set attenuator in each RF channel allows the operator to attenuate the output in 1 dB steps over an 81 dB dynamic range.

The six modulation types (FM by noise, FM by fill, auxiliary FM, linear AM, biphase, and pulse) are independent and may be combined in any way by the operator to modulate the output of an RF channel. In addition, the RF channels are independent, and their outputs may be combined as desired. The variety of modulation types or sources is limited only by equipment availability. For example, only two Wavetek 175 arbitrary waveform generators are available in the system. Each may be used by more than one RF channel, but only two arbitrary modulation waveforms can be generated at a time. This limit is not

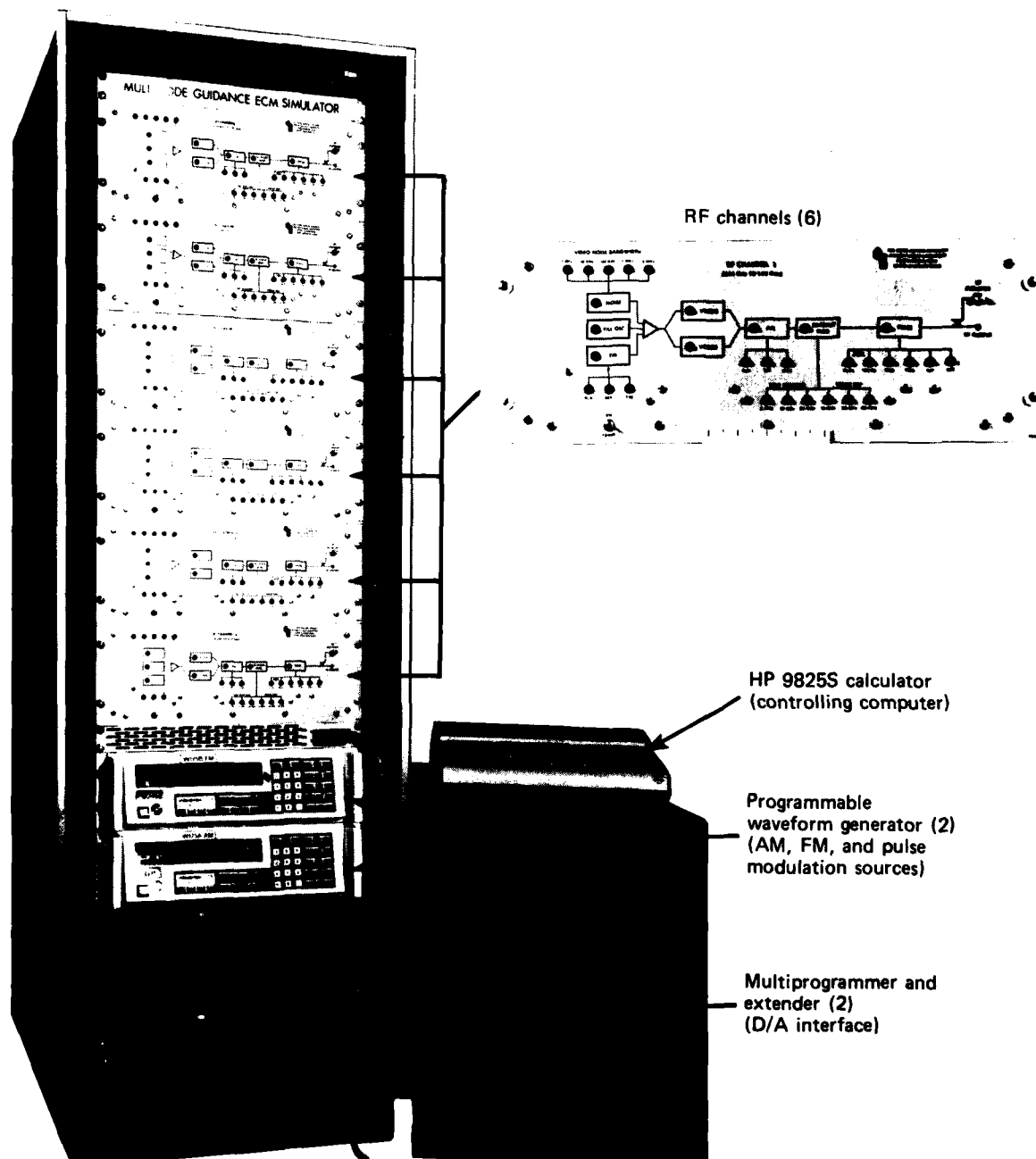


Figure 1 — MMG Low Frequency ECM Simulator.

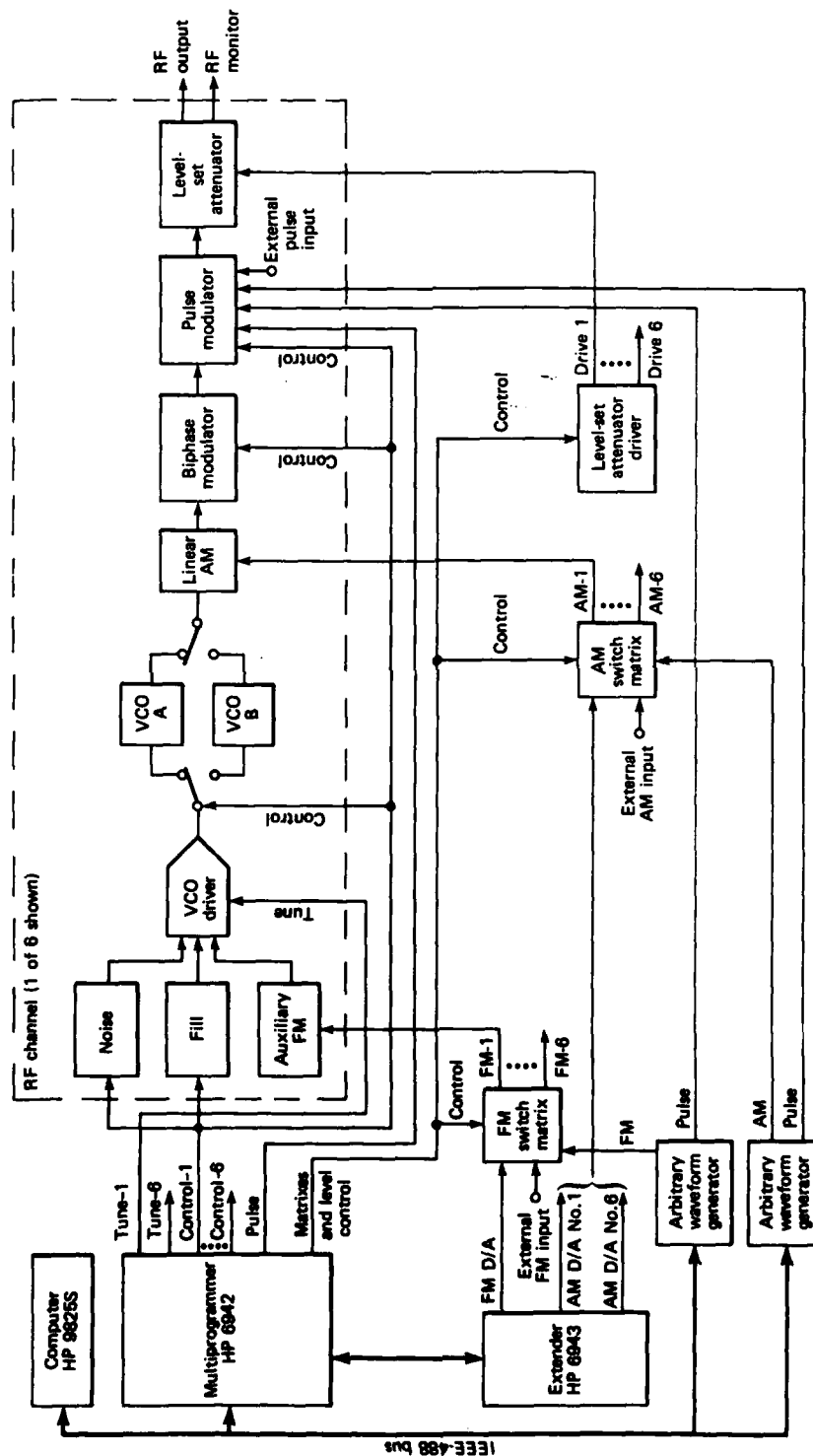


Figure 2 — Block diagram of MMG Low Frequency ECM Simulator.

serious; if more than two waveforms are required, external inputs can be used.

Type I and Type II RF Channels

Each RF channel in the MMG Low Frequency ECM Simulator is a self-contained RF source that requires only AC power, digital control signals, and auxiliary modulation to produce a controlled RF output. Figures 3 and 4 show an RF channel.

There are six RF channels in the system. Three type I channels cover 250 MHz to 1 GHz and three type II channels cover 1 to 4 GHz. Each RF channel contains two single-octave VCO modules, one of which is available at a time, to permit frequency coverage of two octaves.

The functional design and modulation formats are the same for both types of RF channels. A functional block diagram is etched on each front panel (Fig. 5). This diagram shows the four forms of modulation that may be generated in an RF channel. Indicators on the front panel permit an operator to rapidly determine which modulation forms are in use at any time. Each of the modulation forms is independent and any one may be combined with the others to produce complex composite modulations. This allows a

high level of flexibility to simulate not only existing ECM techniques but also postulated ECM threats.

The RF channels are composed of RF, card cage, and power supply assemblies that are removable for service. The card cage contains a set of control cards (one of which is visible in Fig. 4) that provides the digital interface between the controllers and modulation sources, and the RF channel. Each RF channel contains an identical set of control cards. All control, interface, modulation, and power connections are located on the rear chassis (see Fig. 4). The only operator control on the front panel is an RF channel power switch. The RF assemblies contain the RF components depicted on the front panel block diagram (see Fig. 3). The power supply assembly contains all the power supplies needed to operate and control the RF channel.

Frequency modulation of the VCO's is a primary modulation form used in the ECM simulator. One of the principle frequency modulation sources is noise. A Gaussian noise source (Micronetics MSD 1000-2L) is located in each RF channel. Selectable video bandwidths of the noise modulating signal are 1 kHz, 10 kHz, 100 kHz, 1 MHz, or 5 MHz. Either Gaussian or non-Gaussian noise may be used. The amplitude of the FM video signal is adjusted to set the bandwidth of the RF spot. Noise spots covering up to 40% of the VCO bandwidth may be produced.

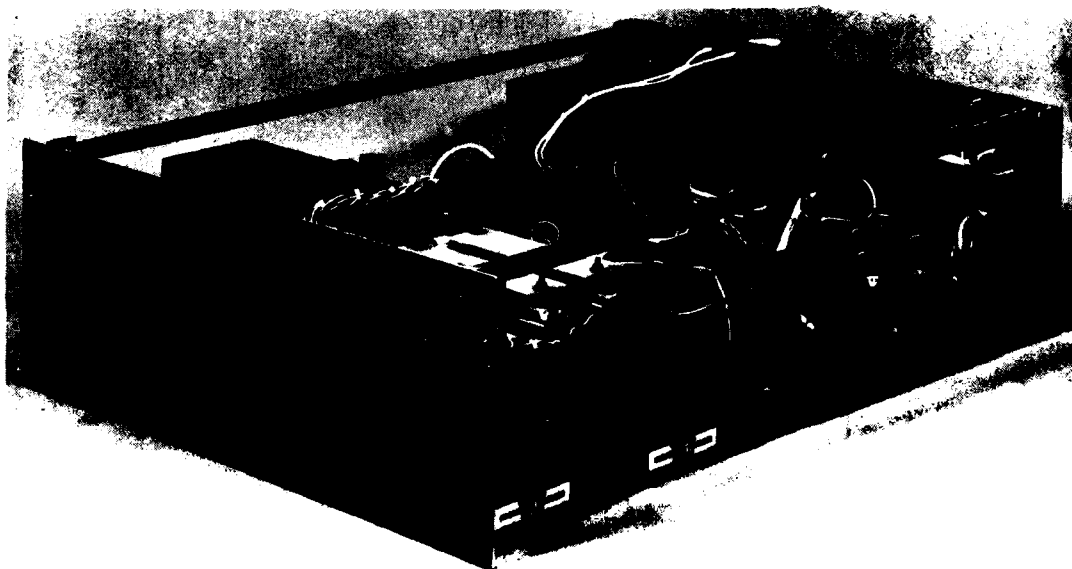


Figure 3 — RF channel, front oblique view.

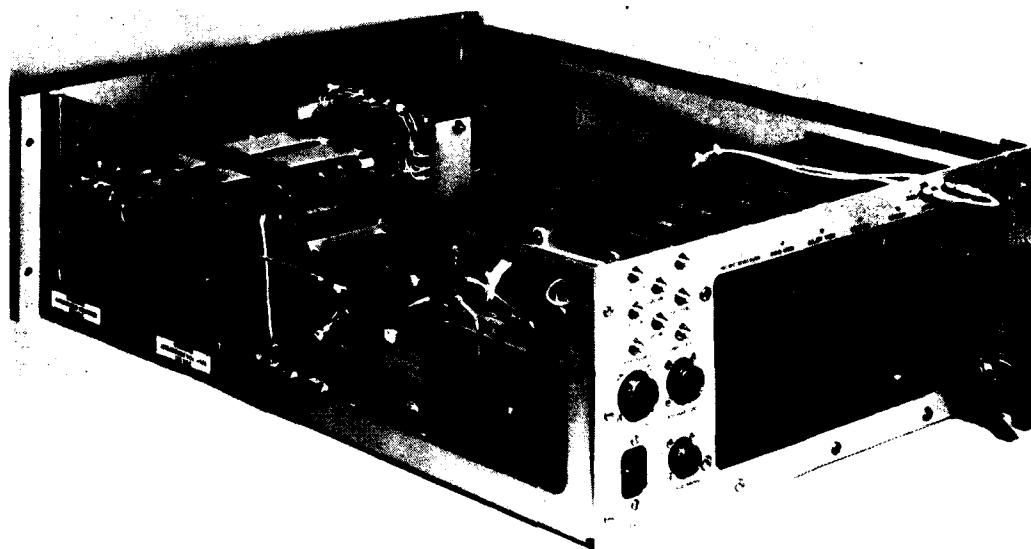


Figure 4 — RF channel, rear oblique view.

A second frequency modulating source available in each channel is a 100 kHz triangular waveform generator. This triangular "fill" signal is used to either spread the RF spot bandwidth or produce an RF spectrum approximately rectangular in amplitude with respect to frequency. The video amplitude of this signal is controllable, to allow generation of the desired RF bandwidth.

A third frequency modulating source is provided through the auxiliary FM inputs, so that an operator may frequency modulate the VCO by one of three different sources. These sources are a digital-to-analog converter located in the HP 6942 multi-programmer, a Wavetek 175 arbitrary waveform generator (which is capable of generating any waveform that can be specified in amplitude as a function of time), and an external function generator with a bandwidth range of DC to over 5 MHz.

The noise, fill, and auxiliary frequency modulating sources can be used individually or combined together to modulate the VCO.

Three modulators (Fig. 5) follow the VCO; these are the amplitude, biphase, and pulse modulators. The amplitude modulator (Anaren 60464 in the type I channels and 60465 and 60466 in the type II channels) enables an operator to program up to 55 dB of amplitude modulation on the RF carrier with a modulating bandwidth of DC to 50 kHz. One of three amplitude

modulating sources may be chosen: a digital-to-analog converter (located in the HP 6943 multi-programmer extender), a Wavetek 175 arbitrary waveform generator; or an external function generator. Amplitude modulation can be used to simulate "range-run-down" programs, antenna pattern characteristics, or multipath effects of a jammer.

The second modulator following the VCO is the biphase modulator, which allows the operator to generate either an RF comb spectrum or a noise-like signal having a power distribution of the form $[(\sin x)/x]^2$. The comb spectrum is generated by shifting the phase of the RF carrier by 0° or 180° , as determined by the levels of a square wave with a 50% duty cycle. Comb spectra with line spacings of 5, 10, or 20 MHz may be produced. The noise-like signal is produced by phase shifting the RF carrier with a long pseudorandom binary sequence instead of a square wave. The bandwidth (between the first nulls) of the noise spot generated is either 10, 20, or 40 MHz. For example, using the comb spectrum, a regular array of narrow noise spots can be generated for an ECM test against a channelized receiver system.

The final modulator (Fig. 5) is the pulse modulator. It is a SPDT switch (Alpha MT-3586A) that allows the RF signal to be blinked at rates up to approximately 1 MHz. The blinking sources can be

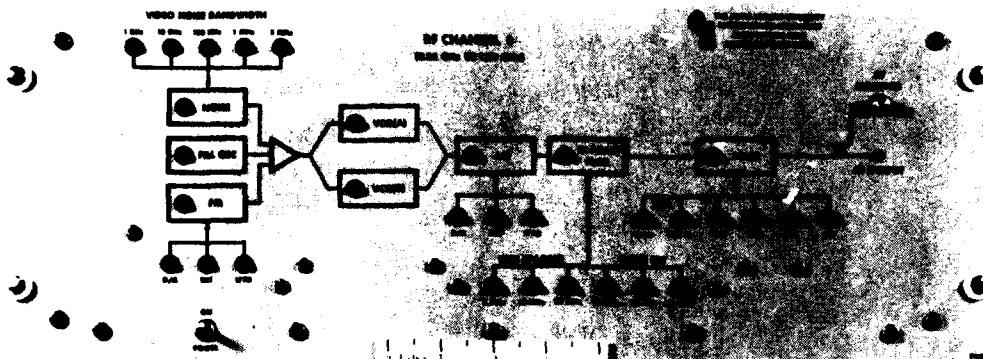


Figure 5 — RF channel front panel.

either an internal 10 or 100 Hz square wave generator, one of two Wavetek 175 arbitrary waveform generators, a timer/pacer card in the multiprogrammer, or an external pulse generator. TTL-level signals are required from either the Waveteks or the external signal source.

The front panel functional block diagram does not show the level-set attenuators in each of the RF channels. These attenuators (HP 8494H and 8495H) allow an operator to control the level of the RF output signal under computer control in 1 dB steps over a range of 81 dB. Since the step attenuators are relay-switched devices, these attenuators would not normally be used for amplitude modulating the signal during a test, but instead would be used to set the RF signal strength to a fixed level at the start of a test.

All six blocks shown in the functional block diagram are independently controlled by the HP 9825 through an HP 6942 and HP 6943 multiprogrammer/extender. In addition, each of the six RF channels is also independently controlled. The channels and all modulation functions within them may be combined as desired, subject only to equipment limitations (e.g., only two Wavetek 175 generators are available) to produce an extremely wide variety of simulated ECM outputs.

Type I and Type II VCO Drivers

The voltage-controlled oscillator (VCO) modules in the RF channels require tuning drive voltages that must be generated by a dedicated driver circuit. The VCO modules in the type I RF channel require a 0 to

+30 V tuning voltage while the type II RF channel VCO modules require 0 to -65 V. In addition, the VCO driver also superimposes a 12 V p-p modulating signal on the DC tuning voltage for frequency modulation (by noise or other waveforms). The bandwidth of this additional modulation is from DC to over 5 MHz.

Figure 6 shows the block diagram of the VCO driver. The differences between the two types of drivers are related to their output drive circuits and are discussed in more detail in Appendix C. The description in this section applies to either type of VCO driver.

The tuning commands to the driver are generated by the HP 6942 digital output card located in the multiprogrammer; they are under the control of the HP 9825S computer. An 8 bit word is used to tune the VCO center frequency. This binary word is converted to a DC voltage within a ± 5 V range by a digital-to-analog converter, amplified, and level-shifted to produce the DC component of the VCO drive voltage.

The noise, fill oscillator, and auxiliary FM signals are added in a buffer, amplified, and added to the DC tuning voltage.

Frequency modulating signals between 100 kHz and 5 MHz are amplified by the noise/FM buffer amplifier and capacitively coupled to the driver output stage (an emitter-follower buffer amplifier). In order to allow the digital controller to rapidly retune the VCO, the value of the final coupling capacitor was chosen to set the low frequency corner at 100 kHz for this modulating signal path.

Modulating signals in the frequency range of DC to 100 kHz are coupled directly from the output of

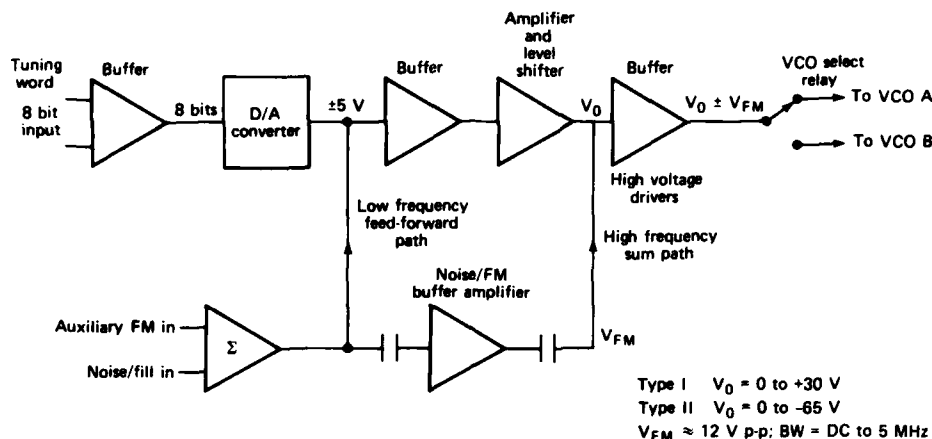


Figure 6 — Block diagram of VCO driver.

the auxiliary FM/fill/noise modulation summing buffer to the input of the D/A buffer where they are added to the D/A tuning voltage. The component values have been selected to keep the composite gain of the feedforward and direct paths flat (within 3 dB) from DC to 5 MHz.

Noise Filter/Fill Oscillator

Two primary frequency modulating signals used by the Low Frequency ECM Simulator are Gaussian (or non-Gaussian) noise and the 100 kHz fill oscillator signal. The noise filter/fill oscillator card provides the buffering and filtering to generate the five noise bandwidths and the 100 kHz triangular fill waveform under computer control. The circuit is described in detail in Appendix D.

Figure 7 is a block diagram of the noise filter/fill oscillator circuits. The fill oscillator is shown at the bottom of the diagram with three BCD control lines. They are used here to turn the fill oscillator on or off. A code 7 (all 1's) will turn the oscillator off; all other input codes will turn it on. These same BCD signals also control the fill attenuator card (described in the following section).

The fill oscillator generates a 100 kHz square wave that is filtered to produce the desired triangular waveshape. The output is buffered to minimize loading effects.

The fill signal is used to frequency modulate the VCO module to either spread the RF bandwidth of a noise spot or to "square-up" the rounded spectrum

that would be generated by frequency modulating the VCO with noise only.

The top half of the block diagram in Fig. 7 shows the noise filters. They are controlled by three BCD lines that command one of the relays (K1 to K4) to close, thus selecting the proper low-pass R-C filter. If all relays are open, the noise bandwidth is 5 MHz; this is referred to as Gaussian noise. Filter bandwidths of 1 MHz, 100 kHz, 10 kHz, and 1 kHz are provided by the filter circuitry to give four "non-Gaussian" noise bandwidths. The noise channel has a buffer amplifier to minimize loading effects on the filter sections.

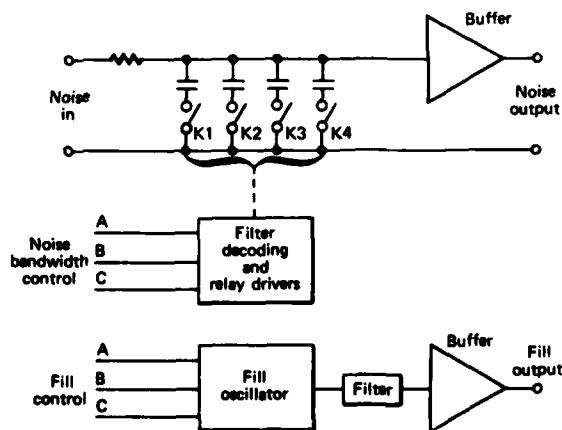


Figure 7 — Block diagram of noise filter and fill oscillator.

The outputs of the filtered noise and the fill oscillator are routed to separate attenuators before being added together. In this way, the RF spectrum width (deviation) can be controlled and also the relative percentages of noise and fill signals used to create a selected RF spotwidth can be changed.

Noise and Fill Attenuators

The amplitude of the noise and fill oscillator signals that frequency modulate the VCO are independently controlled by the HP 9825S computer. This gives an operator the ability to control the bandwidth of the RF spectra and also to vary the relative proportions of noise and fill that are combined to produce the modulating signals.

Figure 8 is a block diagram of the noise or fill attenuator. Two cards are used in each RF channel for the noise and fill attenuation. Since they are identical, no attempt will be made here to distinguish between them. These circuits are described in more detail in Appendix E.

The attenuator card consists of three attenuator sections with attenuation of 6, 12, and 24 dB. Each attenuator section is selected by one of the relays. Since the attenuators are in series, their effects are additive; by selecting the appropriate relays, attenuation values of 0 to 42 dB (in 6 dB steps) can be selected. A buffer following the final attenuator stage minimizes loading effects.

The relay drivers are controlled by three BCD control lines from the multiprogrammer/extender. These lines provide the eight unique states required to generate the 42 dB attenuation range.

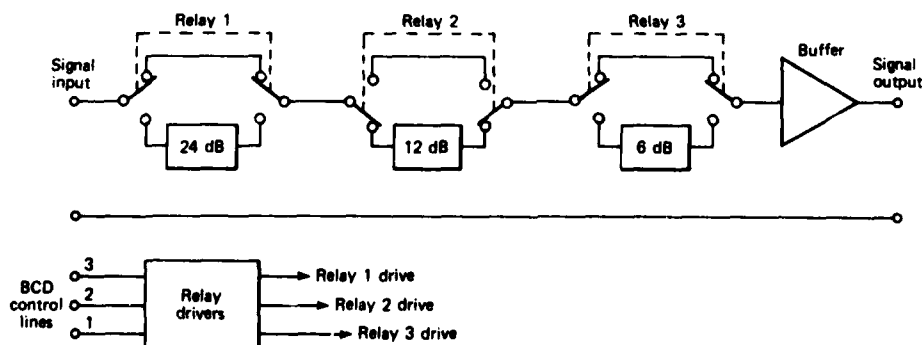


Figure 8 — Block diagram of noise/fill attenuator.

RF Relay Driver

Figure 9 is the block diagram of the RF relay driver. This driver performs two functions: it provides current drive to the VCO select relay and it controls a relay that applies bias voltage to the proper VCO module.

The VCO select relay is a SPDT coaxial relay (HP 8761A) that switches the RF signal from one of the two VCO modules in the RF channel to the RF modulation chain. This relay requires a drive current of one polarity to set the contacts in one direction and a drive current of the opposite polarity to change the contact state. Given a VCO select input signal, the relay driver generates the required current pulse to set the relay in the proper direction for VCO selection. The relay is magnetically latching so it does not require a continuous coil current flow to hold the relay in either state. The drive circuit is described in detail in Appendix F.

The VCO bias relay is a SPDT transfer relay that applies bias to the appropriate VCO module depending on the state of the VCO select line. A high logic state will select VCO A and low state selects VCO B.

Included on the RF relay driver card is a relay that switches primary power to the noise source. The noise source enable input command is generated on the noise filter/fill oscillator card. This control line drives a relay that applies power to the Micronetics Gaussian noise module when a noise modulated signal is required. The noise source is turned off to minimize noise and spurious FM generation when noise modulation is not used.

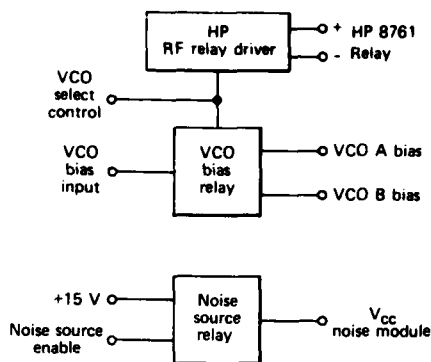


Figure 9 — Block diagram of RF relay driver.

Biphase Modulation Driver

The biphase modulation driver is used to generate either a comb spectrum or a pseudorandom noise spectrum under the control of the HP 9825S computer.

Figure 10 is a block diagram of the driver. A detailed circuit description is given in Appendix G.

Three BCD input lines allow the HP 9825S computer to control the driver modulation modes. They select either the comb or the pseudorandom noise mode and also specify one of three internal clock frequencies. Two states provide for passing the RF carrier (modulation mixer on) or attenuating the carrier by approximately 30 dB (modulation mixer off).

The biphase modulation driver controls a double-balanced mixer (Watkins-Johnson M1J or Summit 1307) in the RF channel with a bipolar current driver that has an output amplitude of approximately 50 mA. The double-balanced mixer passes the RF carrier with no phase reversal for a positive current drive and produces a 180° phase inversion for a negative current drive signal. With no drive, the double-balanced mixer is in its "off" or high attenuation state.

The comb or pseudorandom noise spectra are produced by dynamically driving the double-balanced mixer. If the dynamic current drive is a square wave with a 50% duty cycle, the comb spectrum will result. The tooth spacing on the comb will equal the clock or drive frequency. Clock rates of 5, 10, or 20 MHz may be selected.

When the balanced mixer drive is a long pseudorandom sequence, a noiselike spectrum is produced with a $[(\sin x)/x]^2$ power distribution. The width of

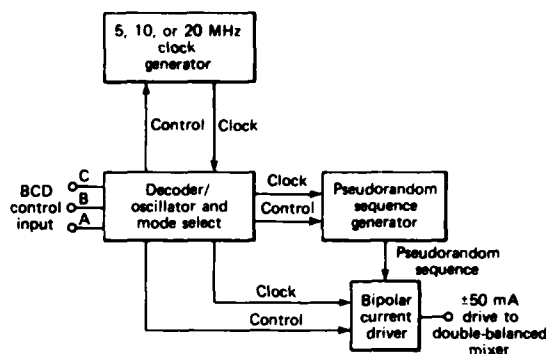


Figure 10 — Block diagram of biphase modulation driver.

the main lobe will be twice the sequence generator clock frequency (in this case 10, 20, or 40 MHz).

Pulse Modulation Selector

The Pulse Modulation Selector is controlled by the HP 9825S computer to select one of eight pulse signals. An SPDT PIN diode switch (Alpha MT-3586A) is used as a pulse modulator in the RF channel; it allows an operator to blink the RF output under program control. The PIN diode switch requires a TTL drive signal; input and output signals associated with this selector are TTL-compatible.

The block diagram of this selector (Fig. 11) shows the inputs to the 8-to-1 multiplexer. Two of the inputs are TTL 1 or 0 logic states that turn the PIN diode switch on or off. Two other inputs are signals from either a 10 Hz or a 100 Hz oscillator located on the selector card.

The remaining four inputs are generated external to the RF channel. Either one of the two Wavetek 175 arbitrary waveform generators can be used to generate a pulse train of an arbitrary duty cycle. A timer/pacer card can generate a 50% duty cycle square wave at up to a 500 kHz rate. The Wavetek 175 and the timer/pacer card are programmed by the HP 9825S computer. An external input is also provided so that other pulse generators may be used as modulation sources.

Three BCD lines control the selection of the eight input signals. These control lines also provide a drive signal that turns on either the 10 Hz or 100 Hz oscillator when it is selected.

A circuit description of this card is presented in Appendix H.

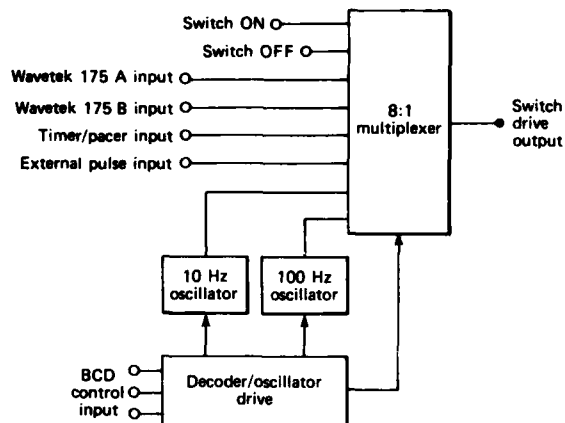


Figure 11 — Block diagram of pulse modulation selector.

AM and FM Modulation Switch Matrixes

The AM and FM modulation switch matrixes are used to connect auxiliary modulation signals to the selected modulator in the RF channel. Two cards contain the AM and FM modulation switch matrixes. These cards are identical and may be interchanged. The difference in function pertains only to the signal sources and their destinations.

The FM signals are routed to the VCO drivers in the RF channels. These FM signals are bipolar with amplitudes up to 2 V p-p. The AM signals (which must be in the 0 to 10 V range) are routed to the

linear amplitude modulators in the RF channels. The signal routing is accomplished via relays on the cards and by the inter-rack cabling. Figure 12 is the block diagram of this card.

The following discussions are pertinent to either the AM or the FM switch matrix card. Each card consists of a 6×3 matrix of relays and associated decoder/driver circuitry. Three signal inputs to the cards come from external signal sources, D/A cards in the multiprogrammer/extender, and two Wavetek 175 arbitrary waveform generators. The signal outputs are buffered (to minimize impedance matching or loading problems) and are routed to the RF channels.

On each card, five control inputs from the multiprogrammer allow an operator to connect one of the three input lines to one or more of the RF channels. Each input line may be connected to any number of RF channels, but only one input may be connected to any channel at a time. The control circuitry on this card is internally latched so that the state of the input to any RF channel will not be affected by state changes made to other RF channels.

The bandwidth of the modulation signal path from the input and through the relay and buffer to the output is approximately 5 MHz, which matches the bandwidth of the auxiliary frequency modulation ports on the VCO drivers. The 3 dB response bandwidth of the amplitude modulators is 50 kHz.

The AM and FM modulation switch matrix cards and the level-set attenuator driver card are mounted in a card cage module located at the rear of the ECM simulator equipment rack. The AM and FM external

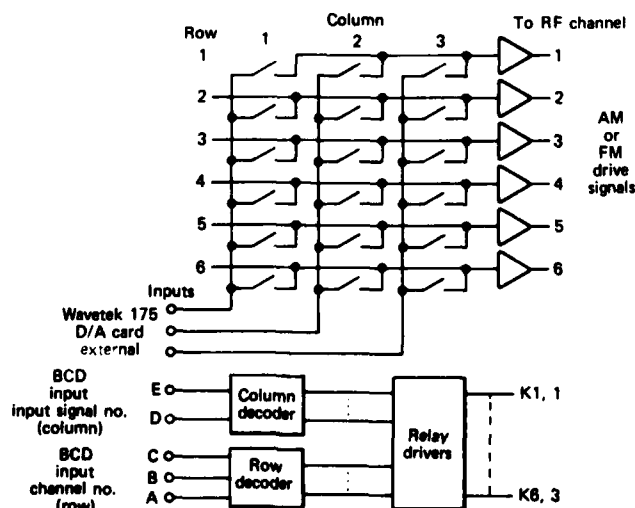


Figure 12 — Block diagram of AM/FM modulation switch matrix.

modulation input ports are located on the rear panel of this module. Three views of this card cage are shown in Figs. 13 through 15.

A detailed circuit description of this card is presented in Appendix I.

Level-Set Attenuator Drivers

Figure 16 shows a block diagram of the level-set attenuator drivers. One card contains six separate driver circuits, each of which drive one of the HP 8494H/8495H attenuator sets in the RF channels.

The HP 8494H attenuator provides 11 dB of attenuation in 1 dB steps using sections weighted 1, 2, 4, and 4 dB. The 8495H attenuator provides 70 dB attenuation in 10 dB steps with 10, 20, and 40 dB section weights. Each of the seven attenuator sections has two solenoids that either insert or remove the attenuation for that section. Therefore, each of the drivers must drive 14 solenoids, as illustrated by driver 3 in Fig. 16. The attenuator sections are magnetically latching so that, once they are set to a state, they will remain there until changed.

The driver circuit is addressed by seven control lines that correspond to the seven attenuator sections. A logic 1 on a control line will cause that attenuator section to be inserted when that driver is enabled and a logic 0 will remove the attenuation.

Three additional BCD control lines address a decoder that generates the six driver enable signals. Only one driver may be enabled at any one time.

The circuit is described in greater detail in Appendix J.

Power Supply Assembly

Each RF channel contains one power supply assembly. A photograph of the type I RF channel power supply assembly is shown in Fig. 17.

Each assembly contains six modular power supplies that provide DC power to all circuits in the RF channel except the level set attenuators.

The module types and functions for the type I and II RF channels are presented below:

Type I RF Channel

<i>Power supply type</i>	<i>Voltage</i>	<i>Current</i>	<i>Function</i>
Power One	+ 5 V	3 A	TTL logic supply
RO Associates (2 each)	± 15 V	750 mA, each side	Analog circuitry, buffers, etc.
Acopian B30FT40	- 30 V	400 mA	VCO bias supply
Acopian B40FT40	+ 40 V	400 mA	V _{CC} for type I VCO driver
Acopian B5FT100	- 5 V	1 A	V _{EE} for type I VCO driver

Type II RF Channel

<i>Power supply type</i>	<i>Voltage</i>	<i>Current</i>	<i>Function</i>
Power One	+ 5 V	3 A	TTL logic supply
RO Associates (2 each)	± 15 V	750 mA, each side	Analog circuitry, buffers, etc.
Acopian B24FT40	- 24 V	400 mA	VCO bias supply
Acopian B70GT30	- 70 V	300 mA	V _{CC} for type II VCO driver
Acopian B5FT100	+ 5 V	1 A	V _{EE} for type II VCO driver

The power supply modules, together with their associated fuses, wiring, and terminal strips, are mounted on an aluminum subchassis that bolts to the main chassis of the RF channel. This feature allows the power supply assembly to be removed intact for servicing if required.

Schematics for these assemblies may be found in Appendix O.

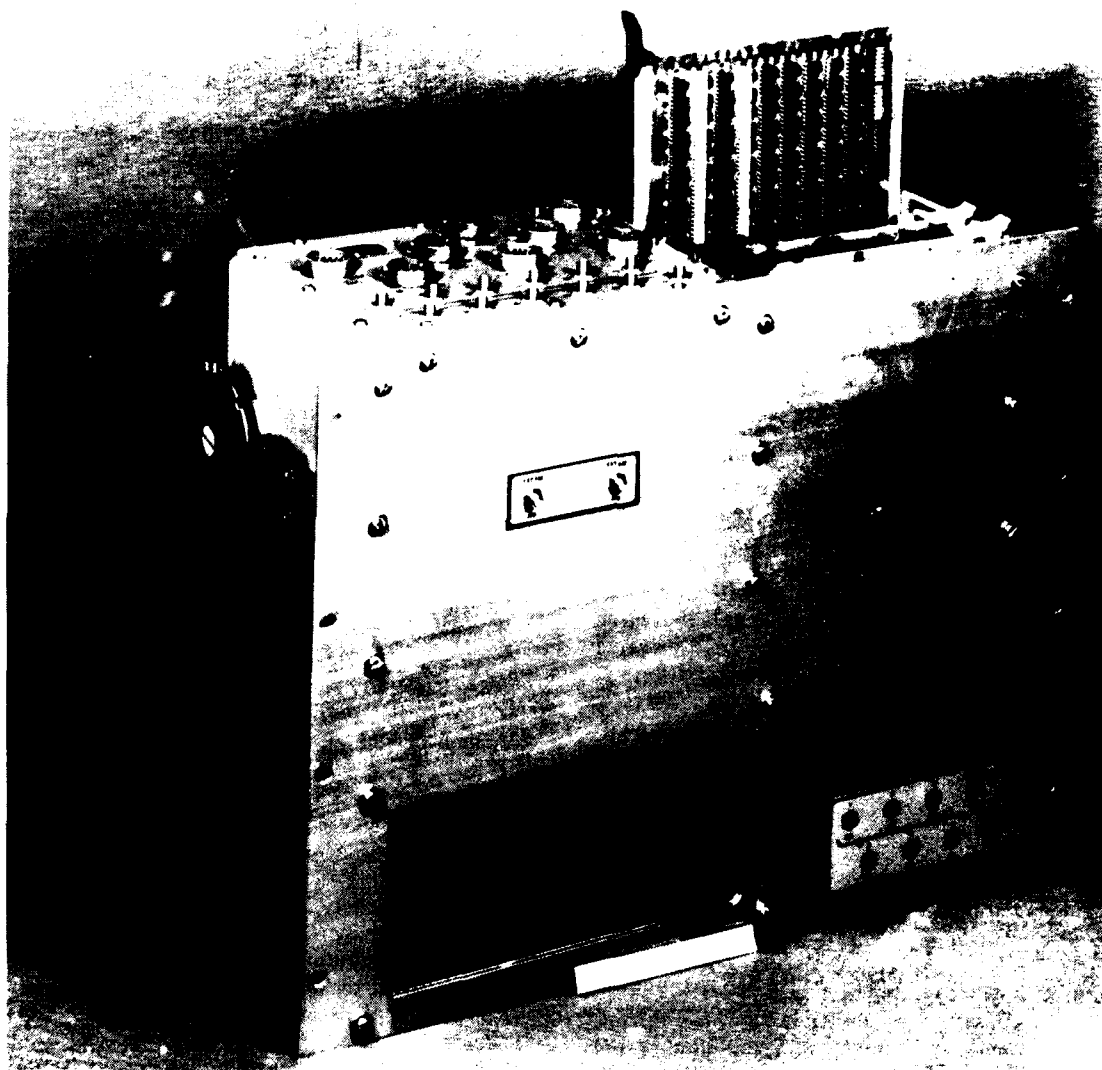


Figure 13 — AM/FM level-set card cage, front view.

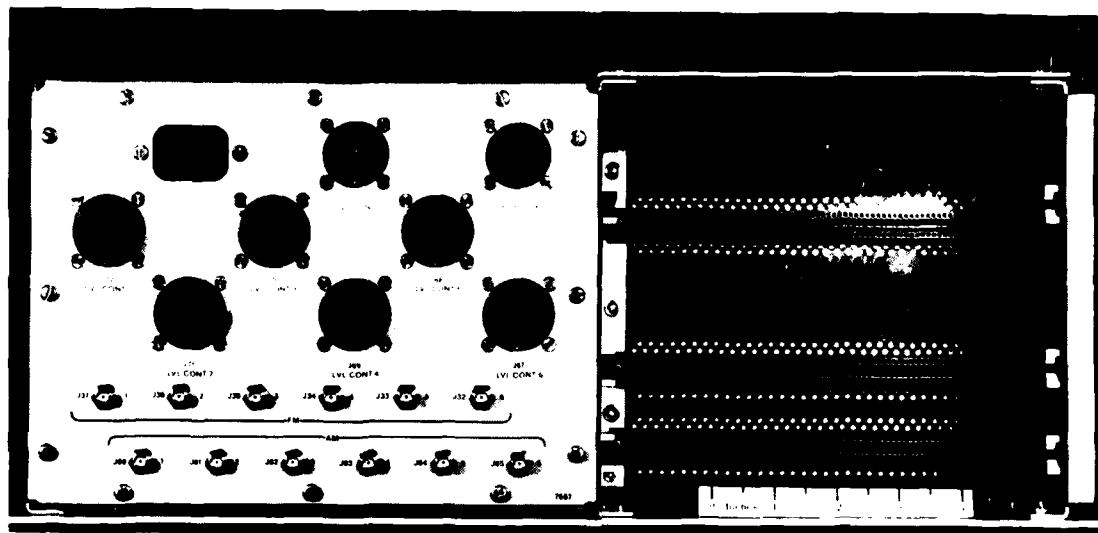


Figure 14 — AM/FM level-set card cage, top view.

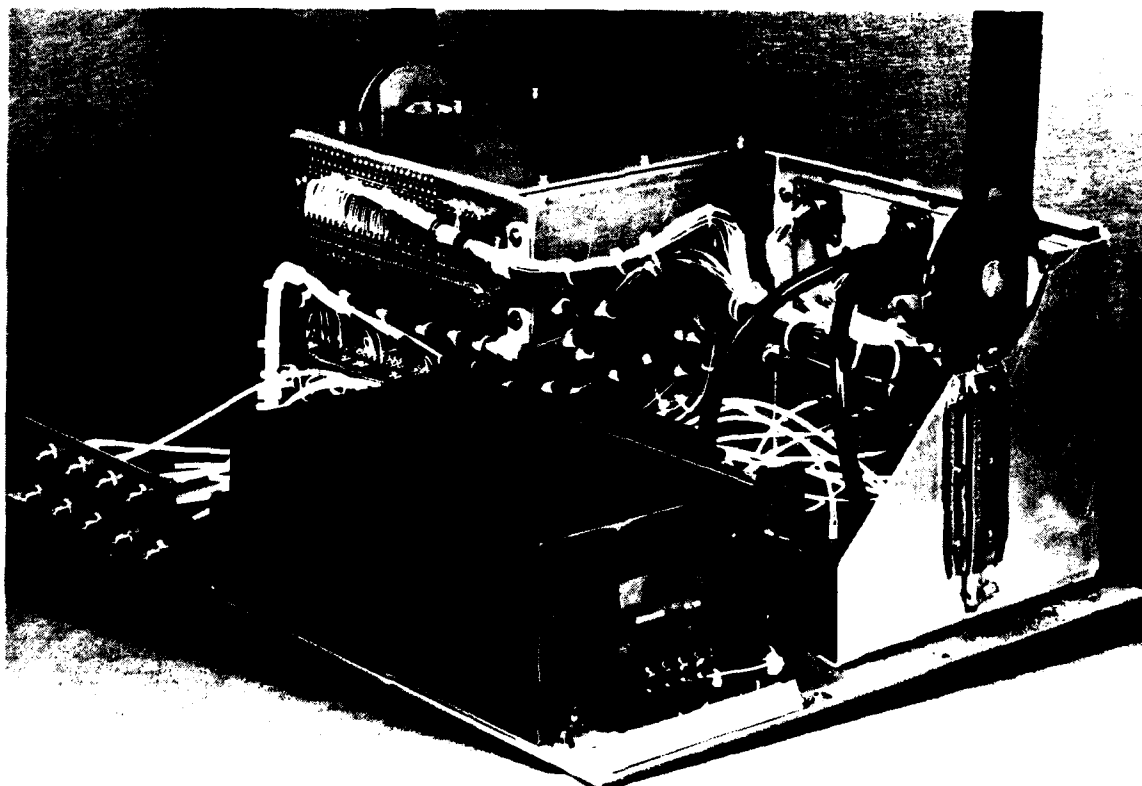


Figure 15 — AM/FM level-set card cage, rear view.

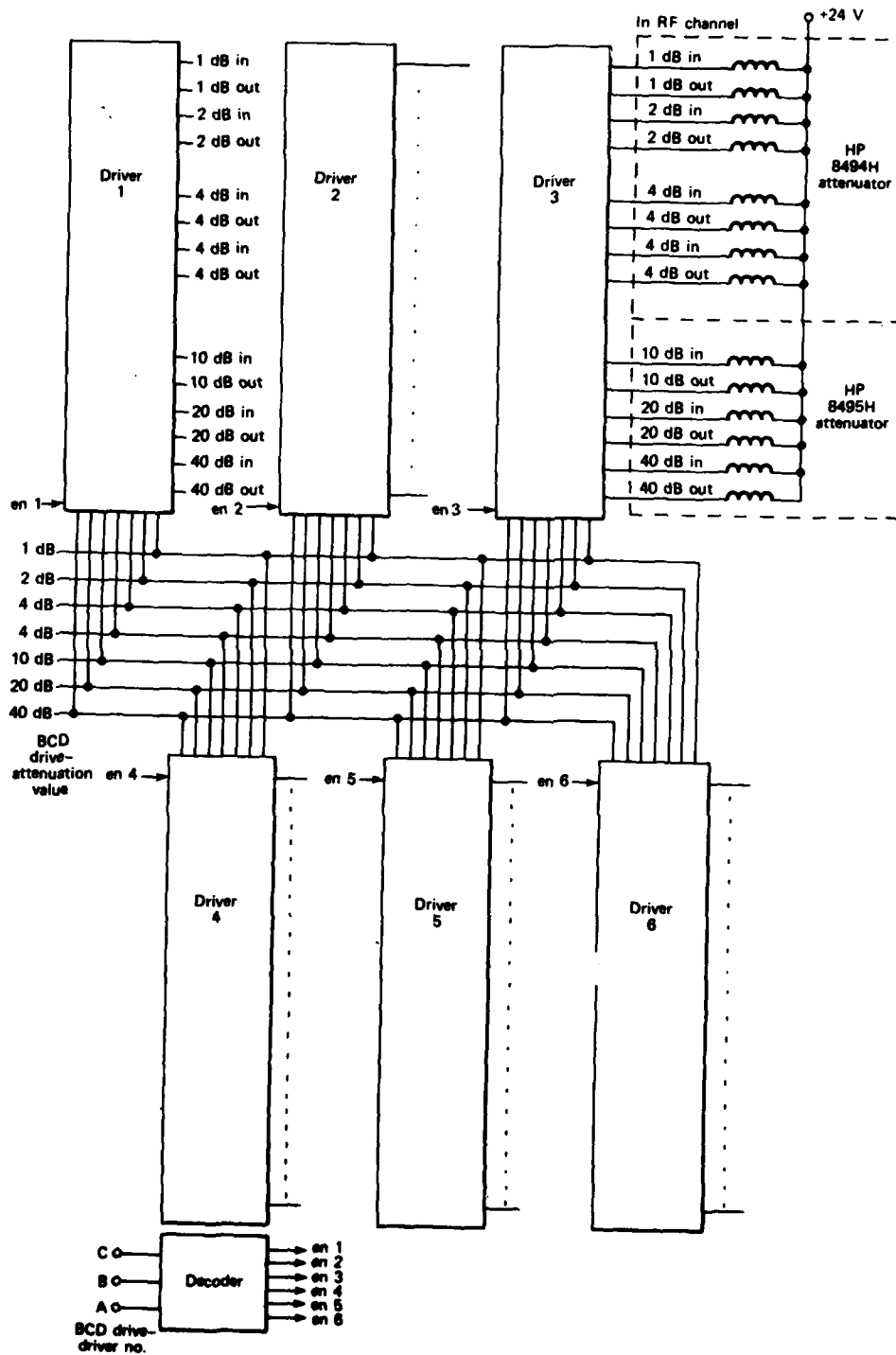


Figure 16 — Block diagram of level-set attenuator driver.

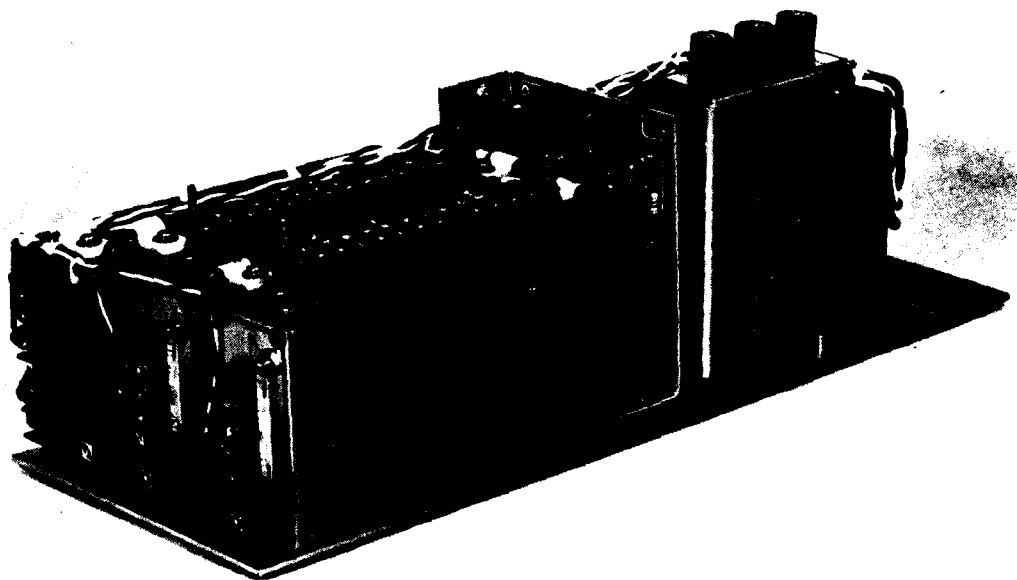


Figure 17 — Type I power supply assembly.

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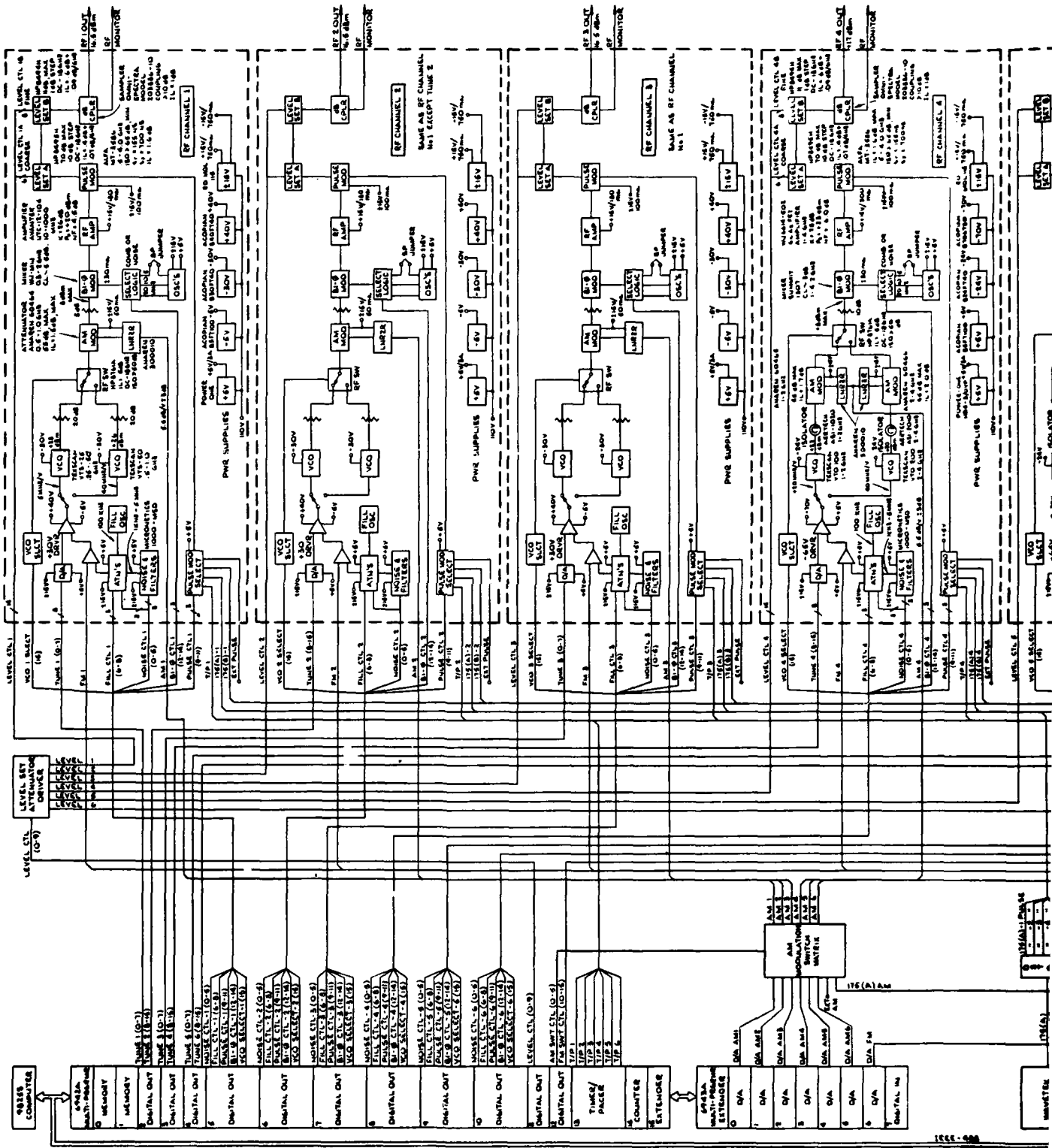
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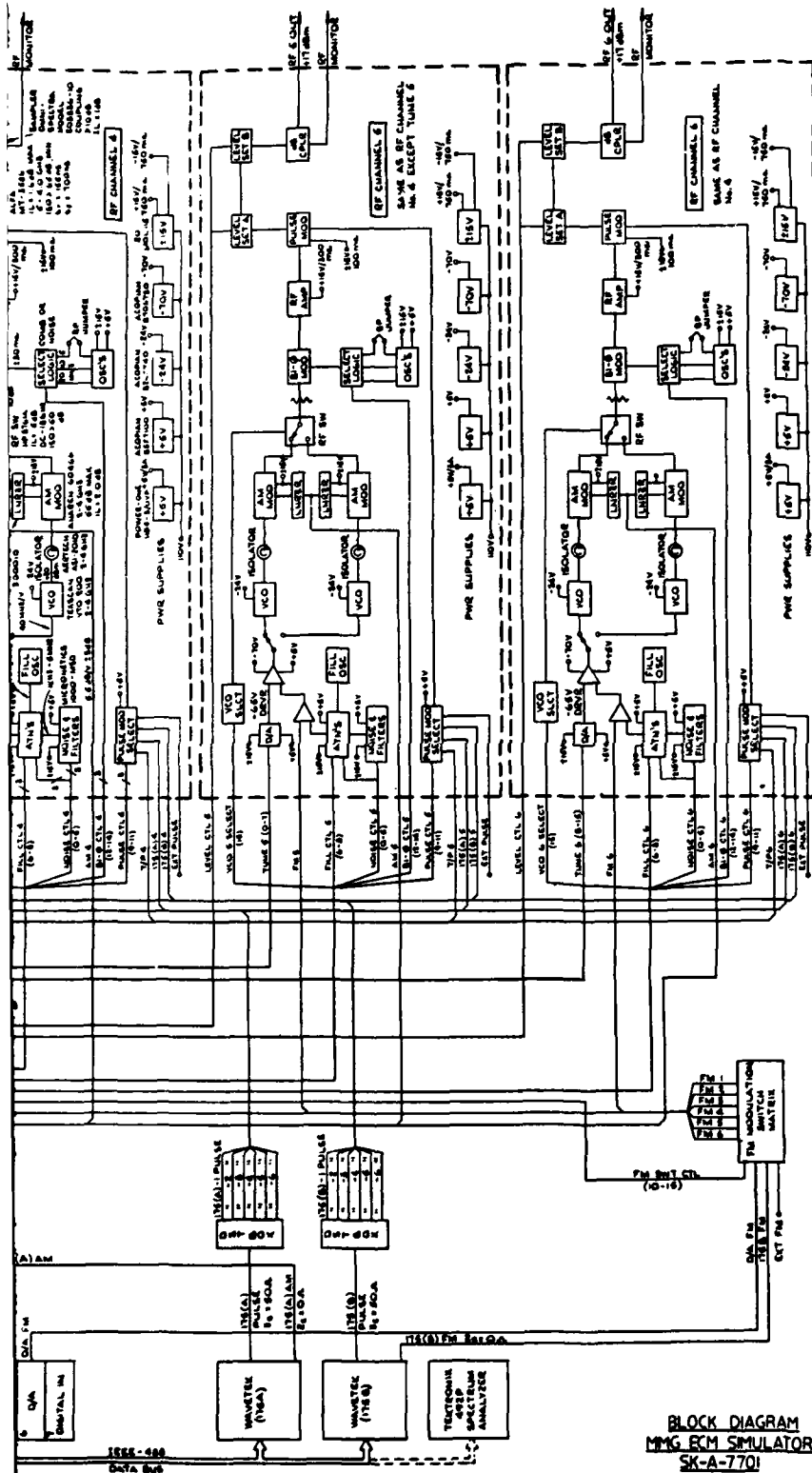


Figure A-1 — Block diagram of MMG Low Frequency ECM Simulator.

APPENDIX A

SYSTEM BLOCK DIAGRAM

Figure A-1 is a system block diagram of the Low Frequency ECM Simulator.

APPENDIX B

TYPE I AND II RF CHANNELS

The RF channel is the fundamental subassembly of the MMG Low Frequency ECM Simulator. It represents a self-contained RF source that requires only power (120 VAC), digital control signals, and auxiliary modulation to generate and control the desired RF spectrum. The ECM simulator has six RF channels designated as either type I or type II. Three type I channels cover the frequency range from 250 MHz to 1 GHz and three type II, from 1 to 4 GHz. Front and rear views of an RF channel are shown in Figs. 3 and 4, respectively. The RF channels are completely self-contained, independent, and (within a type) identical. They may be addressed singly or in any combination under the control of the HP 9825S computer, as specified by an operator.

The RF channel consists of an aluminum chassis approximately 19 in. wide, 27 in. deep, and 7 in. high, on which is mounted all the control logic, RF components, and power supplies required for one RF channel. Figures B-1 and B-2 are block diagrams of

the type I and II RF channels and Figs. B-3 and B-4 are photographs of the type I and II channels with important components identified. The two types of channels are similar, so that only the type I will be described in detail; the type II will be described only in those areas in which it differs.

The RF channel can be divided roughly into three sections. The section nearest the front panel (to the right in the photographs) contains six modular power supplies. These provide power for the logic circuitry, drive circuitry, and RF components in the RF channel with the exception of the level set attenuators. The output voltages are:

1. ± 15 V (from two modules) used for analog buffers, D/A converter, amplitude modulator, and similar circuits.
2. +5 V used for TTL logic circuits.
3. +40 V used as a V_{CC} supply for the type I VCO driver circuit. (For the type II channel this supply is -70 V).
4. -5 V used as a V_{EE} supply for the type I VCO driver circuit. (For the type II this is a separate +5 V supply.)
5. -30 V used for the type I VCO bias supply. (The type II VCO requires -24 V bias.)

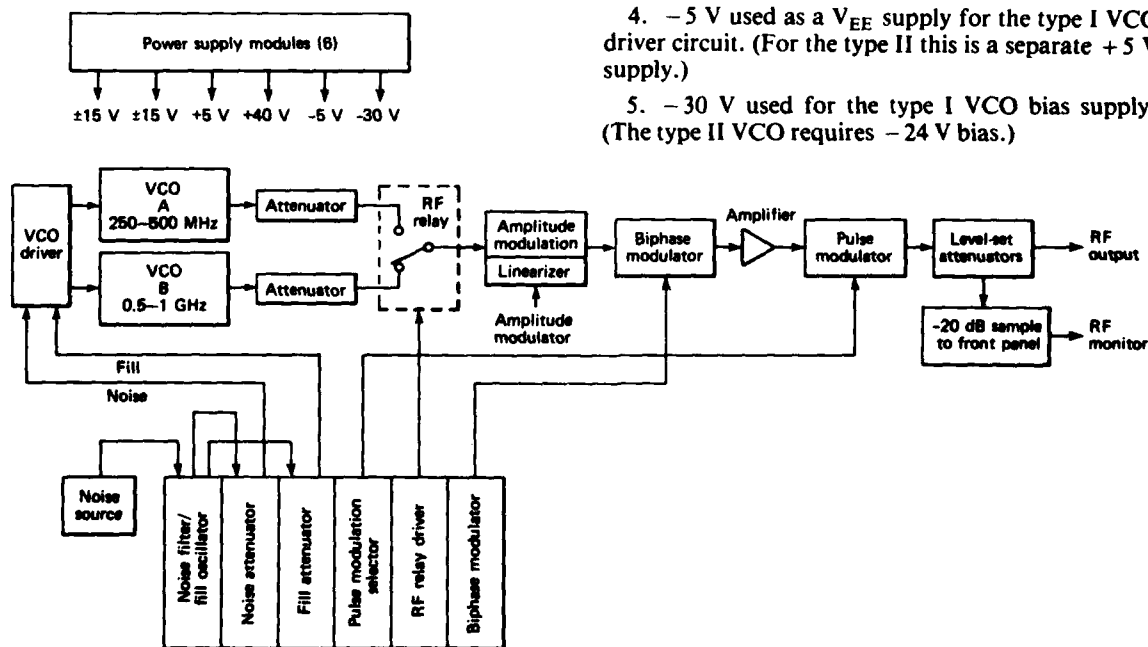


Figure B-1 — Block diagram of type I RF channel.

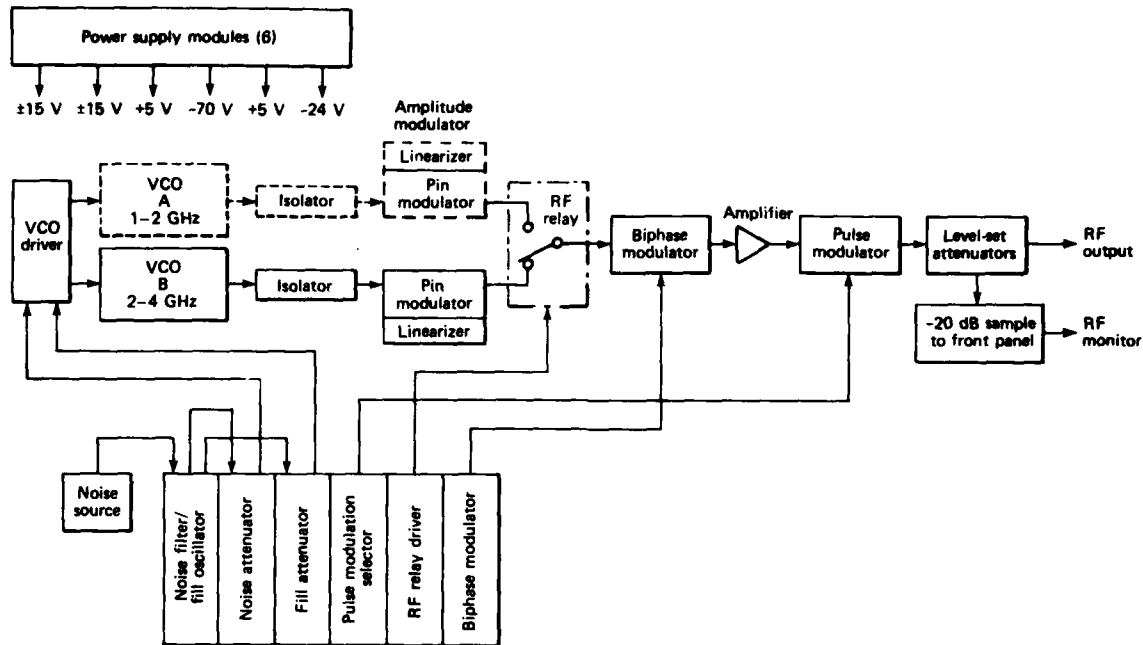


Figure B-2 — Block diagram of type II RF channel.

Power for the linear circuitry in the VCO driver (V_{CC} and V_{EE}) and for the VCO bias voltage is supplied by the three linear Acopian power supply modules. These voltages are isolated from potential noise generated by the logic circuitry and from internally generated noise from a switching type power supply. This minimizes two potential sources of incidental spurious frequency modulation that could appear on the RF output of the VCO. The six power supply modules are mounted on their own subchassis along with associated fuses, terminal strips, and wiring, so as to form a self-contained unit that may be removed intact for servicing.

The rear section of the RF channel is composed of a card cage that holds five wire-wrap circuit cards. These cards act as control interfaces between the HP 9825S/HP 6942 controller circuitry and the RF channel circuits. The functional names of the cards are shown in Figs. B-1 and B-2, together with a representation of their primary signal flow paths. These cards are described in detail in Appendixes D through H. The wiring diagram for this card cage appears in Appendix N as Fig. N-1.

The middle section of the RF channel contains all the RF components, the VCO driver, and the Gaussian noise source (see Figs. B-3 and B-4). The

noise source is a commercial unit (Micronetics 1000 MSD-2L series) that generates noise with a 3 dB video bandwidth of 10 MHz. The noise module will drive a 50 Ω load with a signal whose amplitude is 1 V rms. The VCO driver, used to generate the tuning and modulation signals for the VCO, is described in detail in Appendix C.

The RF chain begins with the VCO modules (see Fig. B-3). In the type I channel, the VCO's have 20 dB attenuators on their outputs to set the RF power level and also to provide a constant load to the VCO's (so as to minimize frequency pulling caused by load variations). The RF relay that follows the attenuators is an HP 8761A SPDT coaxial relay that connects one of the two VCO's to the analog amplitude modulator. The RF relay driver is used to control this relay.

An Anaren 60464 absorptive PIN diode modulator is used to provide amplitude modulation of the RF signal. An Anaren 300010 linearizer aligned to the PIN modulator is also included because the attenuation versus voltage curve to the PIN modulator is nonlinear. This linearizer/PIN modulator combination provides linear attenuation from 0 to 55 dB with a 0 to +10 V input signal. All amplitude modulation signals (whether from the Wavetek 175 arbitrary

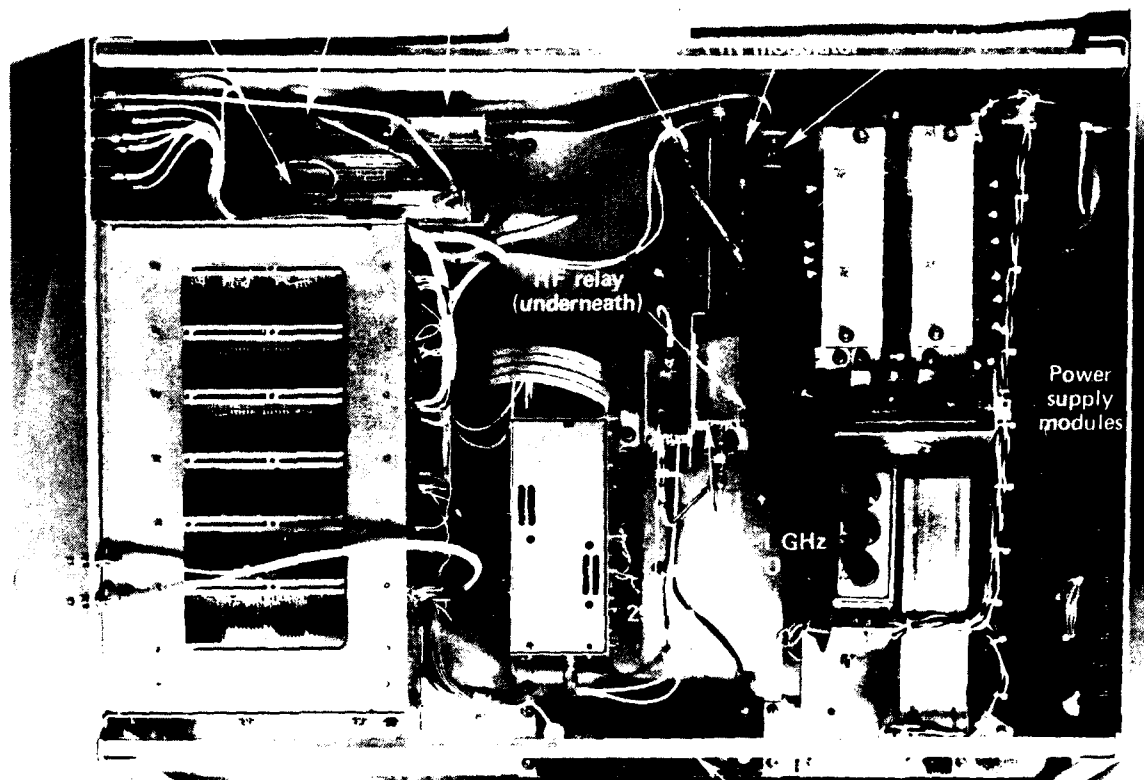


Figure B-3 — Type I RF channel, top view.

waveform generator, the digital-to-analog converter in the multiprogrammer, or an external source) must be in the 0 to +10 V range. The amplitude modulator sensitivity is 5.5 dB/V. The frequency response of the amplitude modulator is from DC to approximately 50 kHz.

The Anaren 60464 PIN modulator used in the type I RF channels is specified by the manufacturer to operate with an RF input frequency range from 500 MHz to 1 GHz; they perform satisfactorily down to 300 MHz. Below 300 MHz the PIN modulator insertion loss versus frequency curve resembled that of a notch or band-stop filter. The maximum attenuation observed was approximately 25 to 30 dB at a frequency between 265 MHz and 285 MHz, for all the units. Figure B-5 is a photograph illustrating this notch phenomenon.

The RF signal then passes through the biphas modulator. In the type I channel the biphas modulator is a Watkins-Johnson MJJ double-balanced mixer, and is driven by a bipolar current driver located on the biphas modulation driver card. The specifications for this device are listed in the components section of Appendix K. A current in one direction into the IF port allows the RF signal to pass through the device with no phase shift while a current in the opposite direction out of the IF port causes a 180° phase reversal between the RF input and output signals. With zero bias current, the mixer is "off" and the RF output is attenuated by approximately 30 dB with respect to the RF input. The biphas modulation driver card drives the mixer with a +50 mA current at rates to 20 MHz. The driver circuit is described elsewhere in this document (Appen-

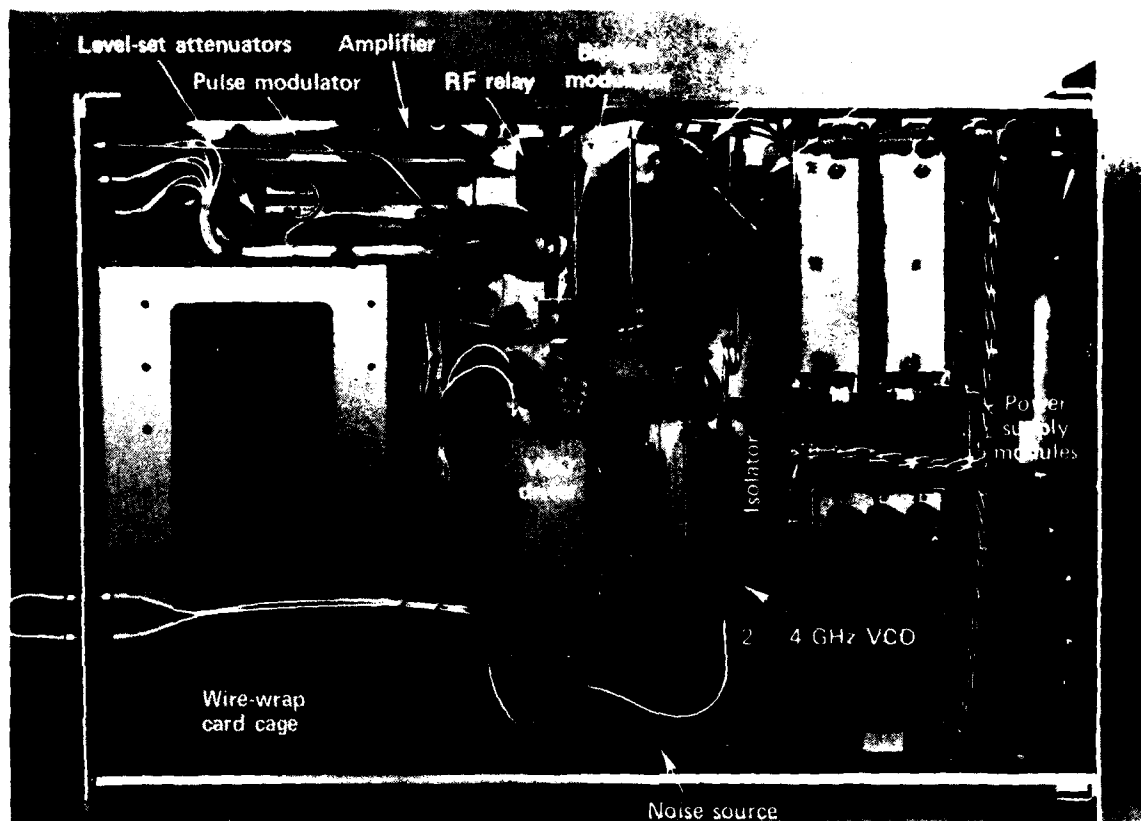


Figure B-4 — Type II RF channel, top view.

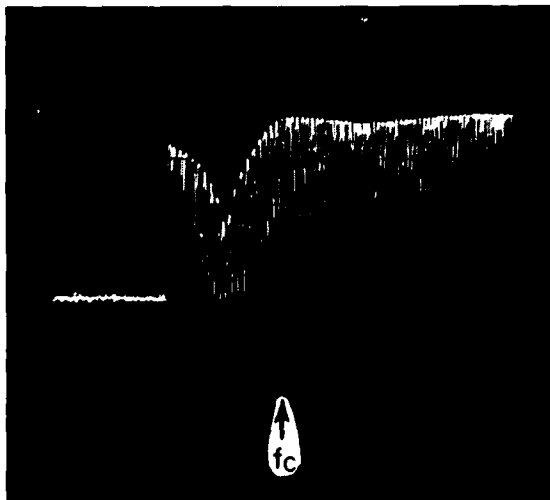
dix G). A fixed attenuator precedes the double-balanced mixer to set the RF level to optimize mixer performance.

Following the biphase modulator, the RF signal in the type I RF channel is amplified by an Avantek UTC-12-104 modular amplifier to a power level of approximately +20 dBm.

Following this amplifier, the RF signal is applied to the pulse modulator, an Alpha MT 3586 SPDT PIN diode switch (used in both type I and II channels). The modulator switch is driven by a TTL-level signal from the pulse modulation selector card and, depending on the drive, passes the RF signal either to the output or into a 50 Ω dummy load. This switch and its driver permit an operator to blink the RF output on and off at several fixed or arbitrary pulse rates and duty cycles. The pulse modulation selector is described elsewhere in this document (Appendix H). The switch provides at least 65 dB of isolation in its off state.

The RF signal from the pulse modulator is applied to the level-set attenuators. These are an HP 8495H step attenuator and an HP 8494H step attenuator connected in series. The attenuators are relay operated and controlled by the level-set attenuator driver (described in Appendix J) located in the AM/FM/Level-Set card cage. The relay switches in the step attenuators are magnetically latched so that power is required only to change state. The HP 8495H attenuator has a 70 dB range in 10 dB steps and the HP 8494H attenuator has an 11 dB range in 1 dB steps for a series combination of 81 dB in 1 dB steps. The same attenuator assembly is used in the type I and II channels.

After the attenuators, the RF signal is routed to a rear panel output connector and to a 20 dB coupler that provides a front panel sample of the RF signal. The RF wiring in both types of channels is semirigid coaxial cable to minimize loss, spurious radiation, and cross-coupling between heads.



Notes: Spectrum analyzer photograph
Vertical scale = 10 dB/cm
Horizontal scale = 20 MHz/cm
 $f_c = 280$ MHz
Multiple scans have been integrated
to show frequency detail.

Figure B-5 — "Notch filter" phenomenon caused by amplitude modulator.

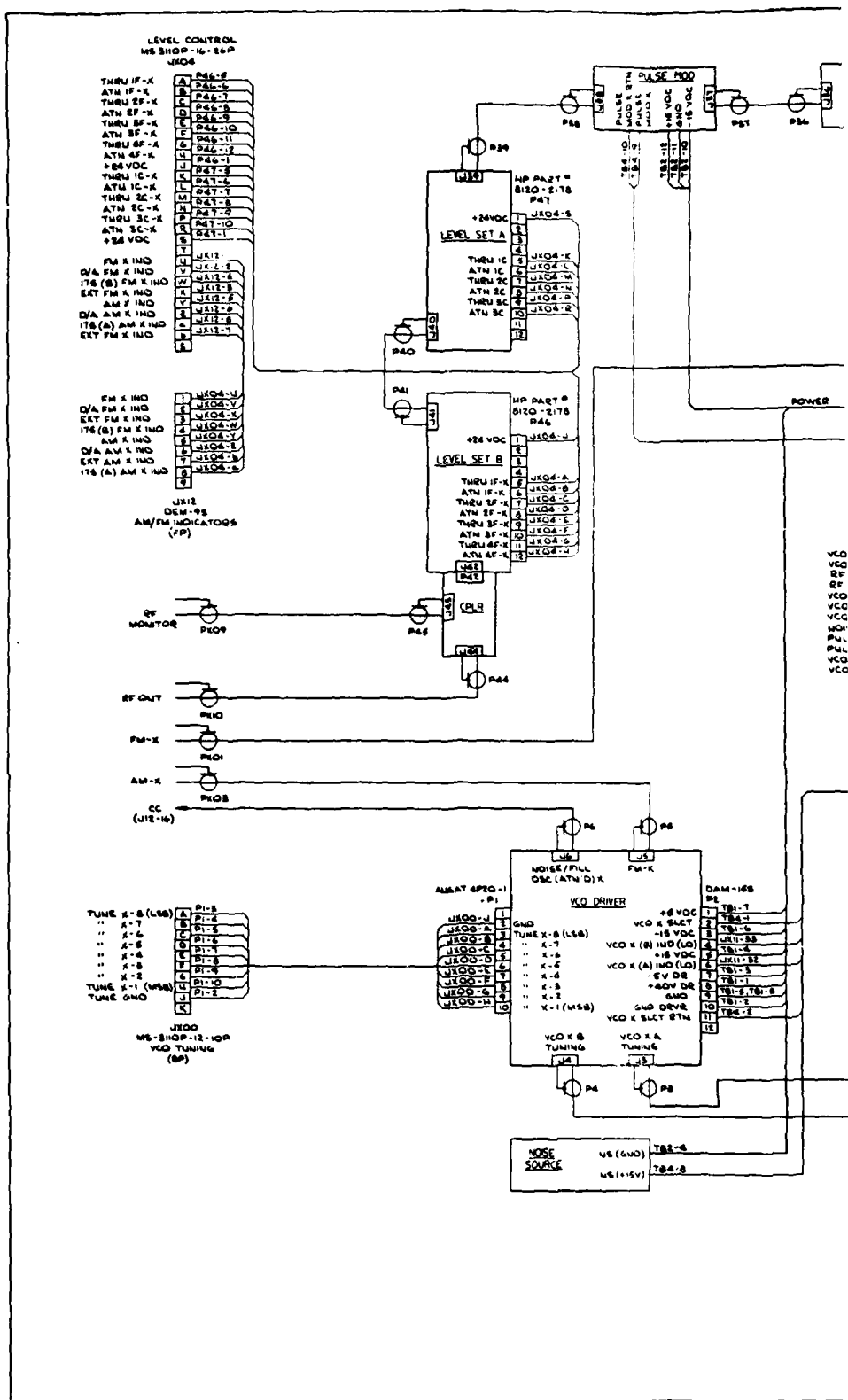
The RF circuitry in the type II channel is similar to the type I; it uses the same types of modulators, the

differences being dictated by the frequency coverage of the specific modules. The wiring diagrams for the type I and type II channels are shown in Figs. B-6 and B-7.

In Figures B-2 and B-7, each VCO in the type II channels is followed by an isolator (to minimize frequency pulling) and an amplitude modulator/linearizer. Two isolators and modulators were needed since these components operate over only one octave of frequency. (The components associated with VCO A (1 to 2 GHz coverage) are shown in dotted lines (they were not initially purchased for the type II RF channels). Incorporation of these components was included in the packaging design, however, and they will be installed during 1982.) Each PIN modulator requires its own linearizer, since these units are adjusted as pairs by the manufacturer to produce a linear attenuation curve of 5.5 dB/V.

In the type II channels, the HP 8761A RF relay follows the amplitude modulators. All the RF components beyond this point are sufficiently broadband to cover the desired 1 to 4 GHz frequency band.

The biphase modulator and amplifier in the type II channels perform exactly the same functions as in the type I channels. Their model numbers and relevant specifications are listed in the components description (Appendix K). All the other components in the RF signal path of the type II RF channels are the same as those in the type I RF channels.



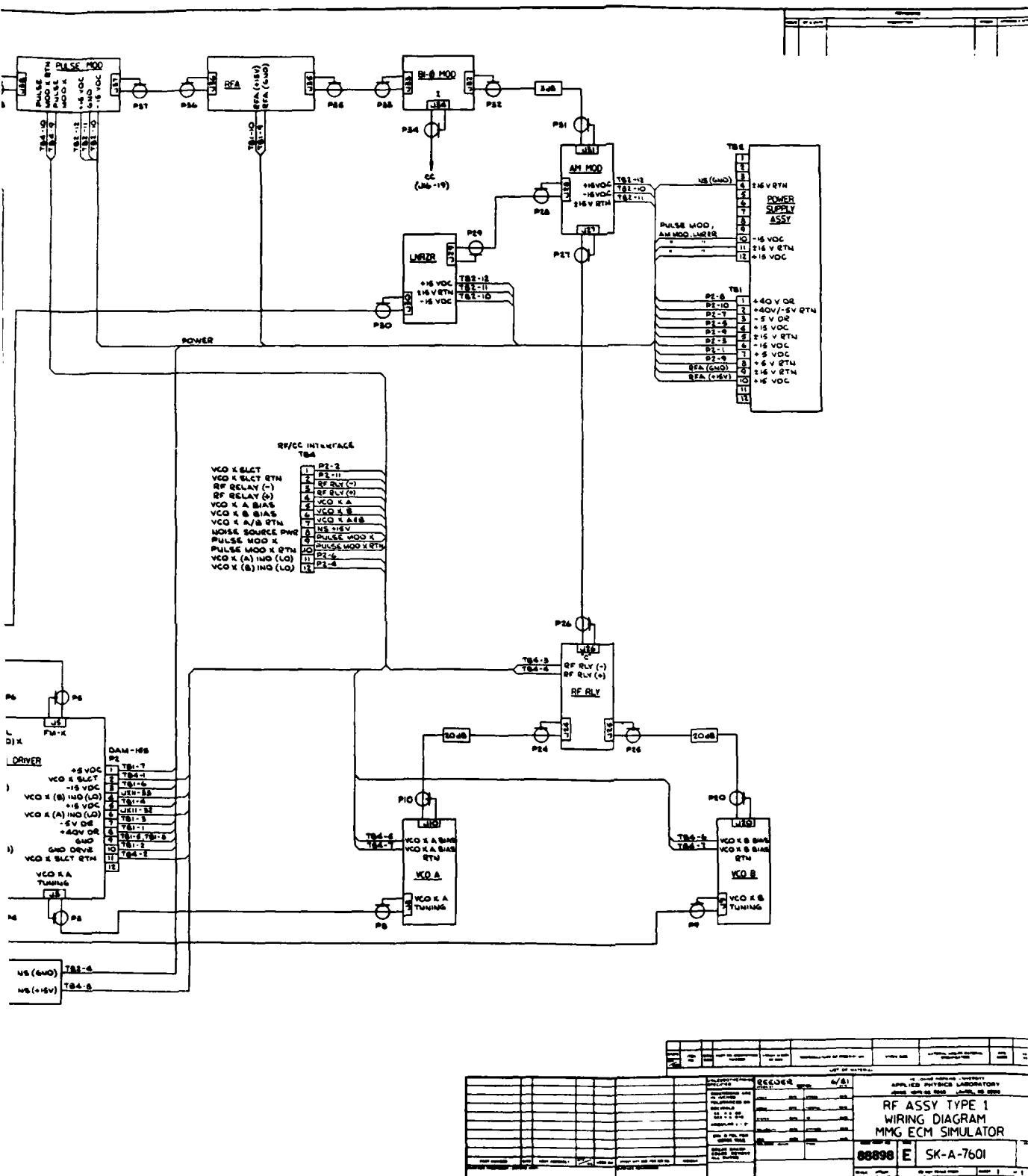
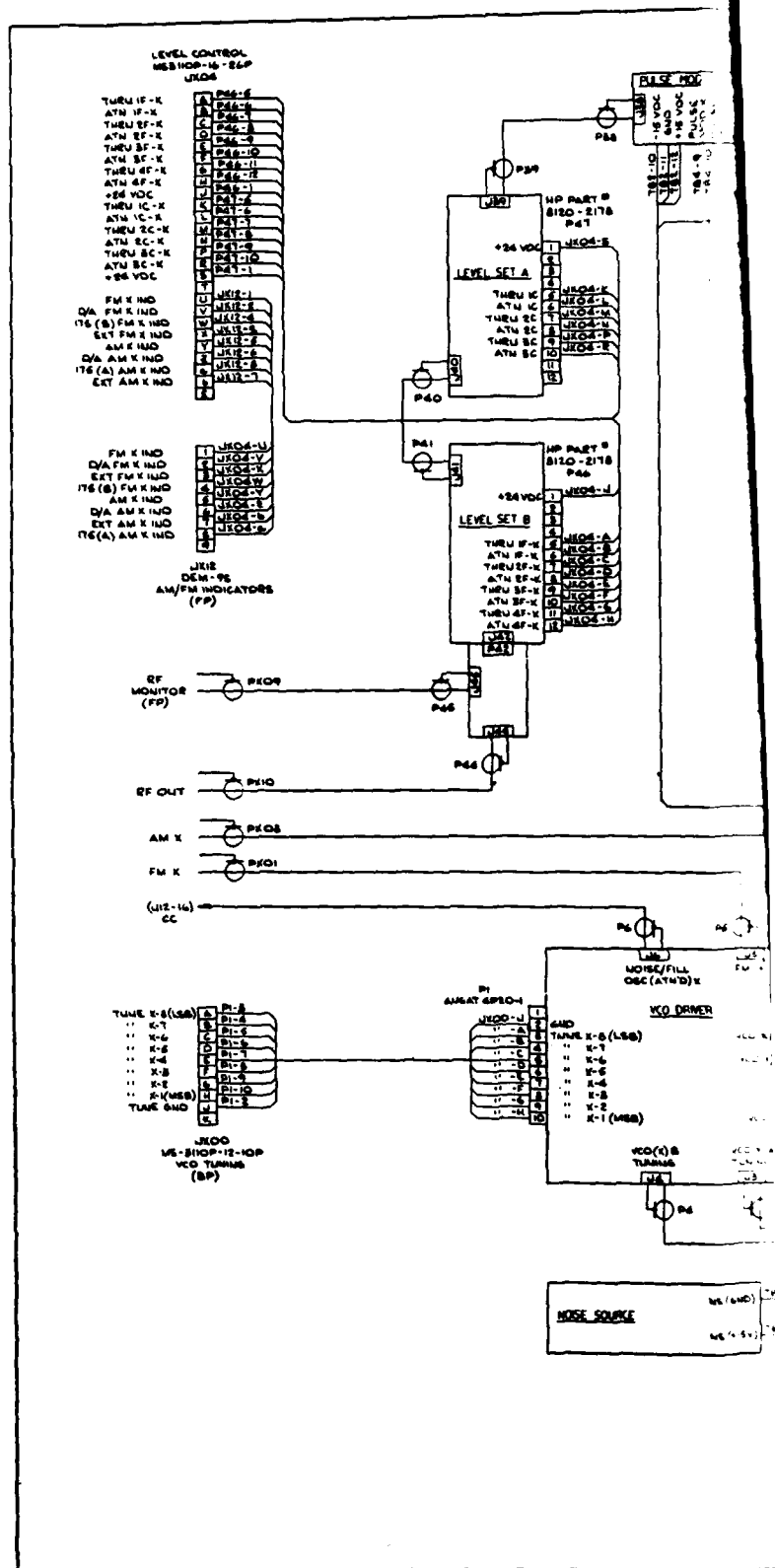


Figure B-6 — RF assembly, type I wiring diagram.



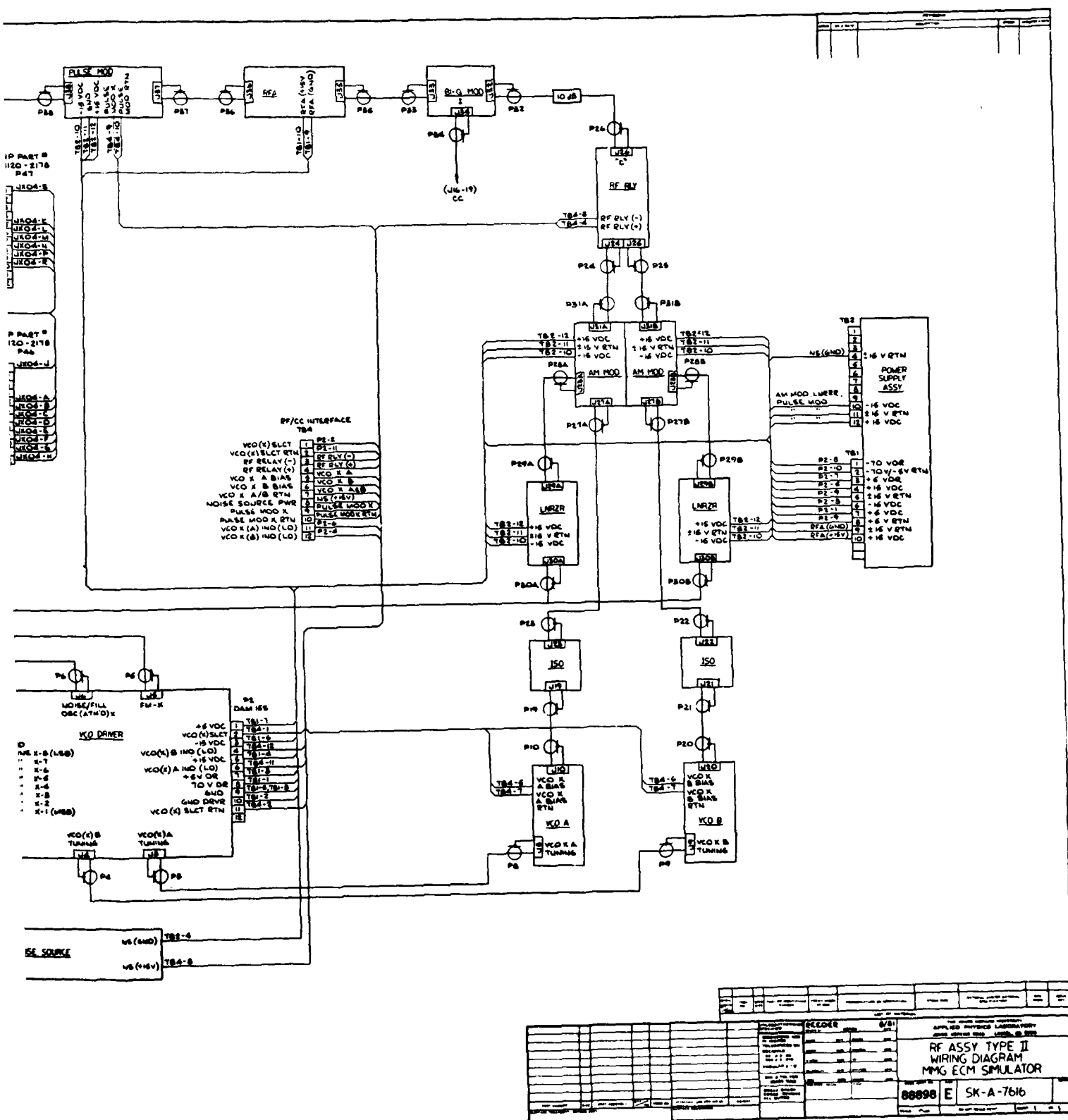


Figure B-7 — RF assembly, type II wiring diagram.

APPENDIX C

TYPE I AND TYPE II VCO DRIVERS

Figure C-1 is a block diagram of the VCO driver. This diagram applies to both the type I and type II drivers, which differ primarily in their output drive stages. The type I drivers have a 0 to +30 V output range for tuning the VCO, and the type II drivers have a 0 to -65 V output range. Both drivers are capable of superimposing on the DC tuning voltage a 12 V p-p signal with a 3 dB bandwidth in excess of 5 MHz. This superimposed voltage provides the frequency modulation signals required to simulate jammers.

This Appendix will describe the design of the type I driver in detail. The type II design will be discussed only in those areas that differ from the type I design.

The type I driver (see Fig. C-2) is designed to convert an 8 bit digital word from the HP 9825S computer into an analog voltage in the 0 to 30 V range. The digital word is entered through J1 and buffered by inverters U1 and U2 before being converted to an analog voltage in the ± 5 V range by U3. The output of U3 is buffered by the unity gain amplifier composed of U4 and U5. The D/A converter U3 is set in a complementary offset binary mode so that an all zero code (all 1's at J1) will produce a +5 V output at TP1.

The ± 5 V output of the D/A converter is ampli-

fied and level shifted by Q1 to provide the desired 0 to 30 V output range. This signal is buffered by Q2 to provide sufficient drive to the VCO tuning port. The frequency response of this signal path (from U1 to Q1) is from DC to nearly 100 kHz, which is more than adequate to follow changes in the digital tuning word from the HP 9825S.

Inputs J5 and J6 provide the rapid time-varying signals used to frequency modulate the VCO. Auxiliary FM signals from J5 are summed with noise and fill oscillator signals from J6 by a resistive summing network preceding buffer U7. The frequency response of the FM signal path extends from DC to slightly over 5 MHz. DC and low frequency coverage is provided by a feedforward path through R36 to U4, U5, and Q1. This feedforward path allows true DC coupling of the external FM signals and, since the feedforward path has a frequency response to nearly 100 kHz, permits the use of a smaller value of coupling capacitor (C8) between U8 and Q2. The smaller value of C8 is desirable since it minimizes capacitive loading of Q1 and permits the DC component of the VCO tuning voltage to respond rapidly to step changes commanded by the HP 9825S. The noise/FM buffer composed of Q3, Q4, and U8 provides the high frequency path for the noise/FM signal. The composite frequency response of the two

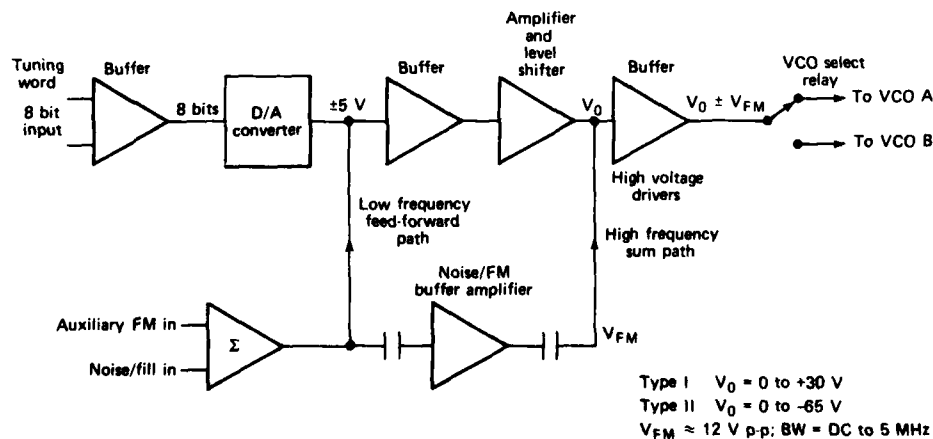
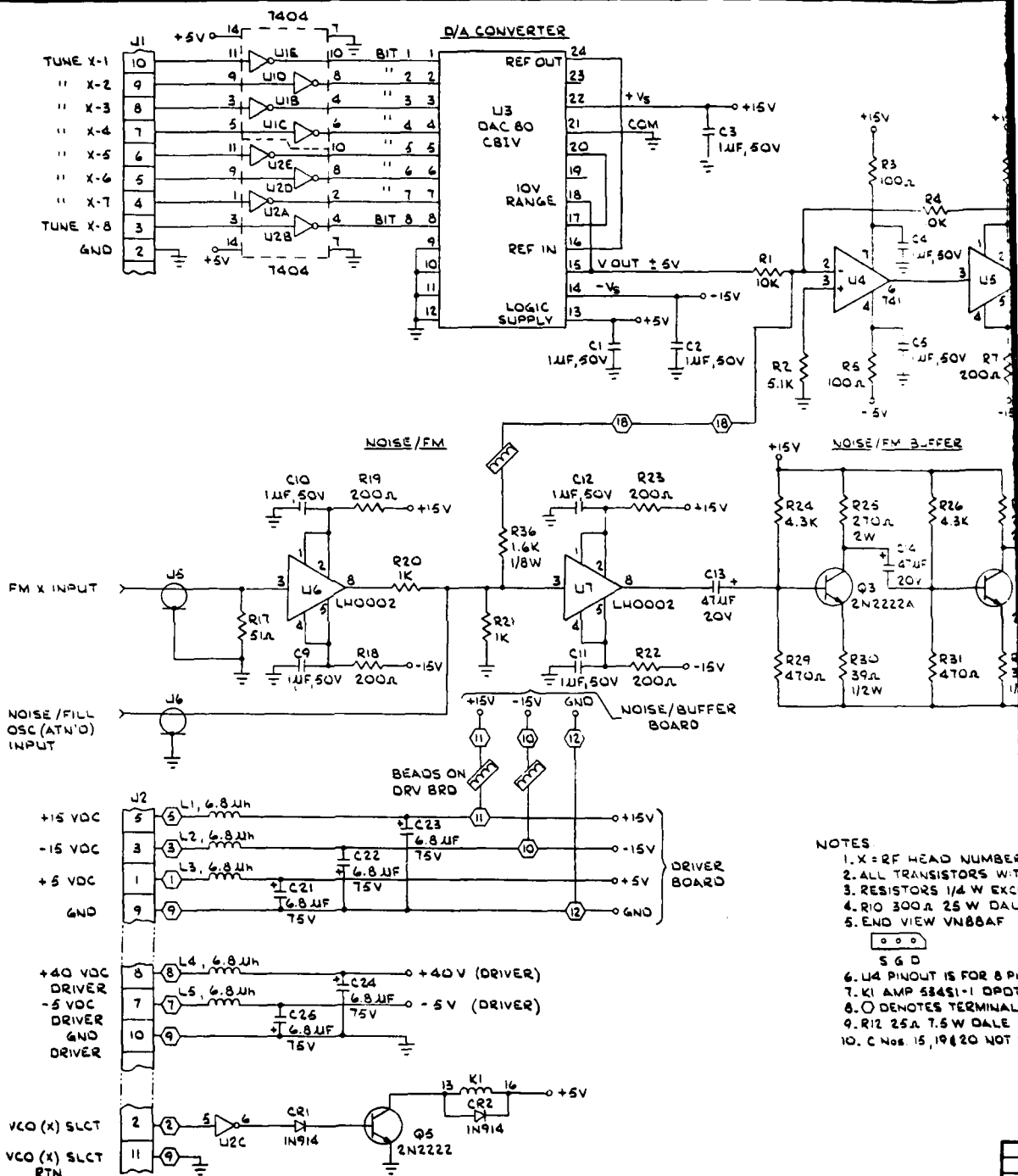
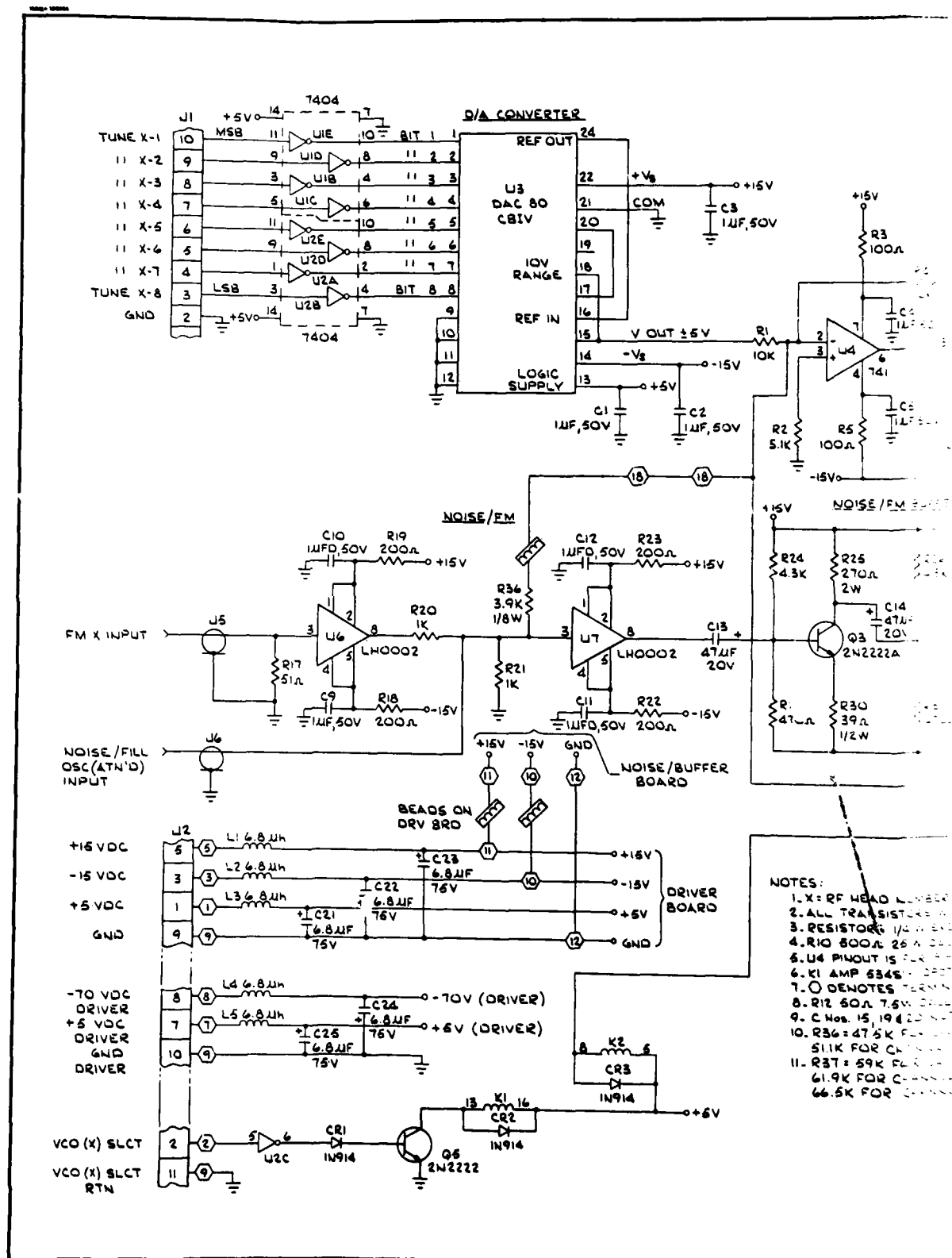


Figure C-1 — Block diagram of VCO driver.





REVISIONS				
REV	DATE	DESCRIPTION	BY	APPROVED DATE
1	02/08/82	ADDED K2, CR3, R36, R37		02/08/82

The schematic diagram illustrates a PLL FM transmitter circuit, divided into three main functional blocks: NOISE/FM BUFFER, TUNE X (ANALOG), and a final output stage.

NOISE/FM BUFFER: This section generates a noise signal for frequency modulation. It features two 741 op-amps (U4, U5) and two LH0002 comparators (U6, U7). The circuit is powered by a 15V supply and a 5V DRIVER. Key components include resistors R3 (100Ω), R4 (1K), R5 (100Ω), R6 (200Ω), R7 (200Ω), R8 (1K), R9 (3.3K, 2W), R10 (500Ω, 25W), R11 (220Ω, 1/2W), R12 (50Ω, 7.5W), R13 (10K, 1/2W), R14 (10K, 1/2W), R15 (1.2K, 10W), R16 (1K), R17 (10K, 1/2W), R18 (10K, 1/2W), R19 (10K, 1/2W), R20 (10K, 1/2W), R21 (10K, 1/2W), R22 (10K, 1/2W), R23 (10K, 1/2W), R24 (10K, 1/2W), R25 (270Ω, 2W), R26 (4.3K), R27 (270Ω, 2W), R28 (200Ω), R29 (200Ω), R30 (39Ω, 1/2W), R31 (470Ω), R32 (39Ω, 1/2W), R33 (6.2K), R34 (1K), R35 (200Ω), R36 (10K, 1/2W), R37 (10K, 1/2W). Capacitors include C1 (100nF, 50V), C2 (100nF, 50V), C3 (100nF, 50V), C4 (100nF, 50V), C5 (100nF, 50V), C6 (100nF, 50V), C7 (100nF, 50V), C8 (100nF, 50V), C9 (100nF, 50V), C10 (100nF, 50V), C11 (100nF, 50V), C12 (100nF, 50V), C13 (100nF, 50V), C14 (100nF, 50V), C15 (100nF, 50V), C16 (100nF, 50V), C17 (100nF, 50V).

TUNE X (ANALOG): This section generates a voltage-controlled oscillator (VCO) signal. It uses a 2N5680 JFET (Q1) and a 2N5480 JFET (Q2). The circuit is powered by a 15V supply and a 5V DRIVER. Key components include resistors R1 (100Ω), R2 (100Ω), R3 (100Ω), R4 (1K), R5 (100Ω), R6 (200Ω), R7 (200Ω), R8 (1K), R9 (3.3K, 2W), R10 (500Ω, 25W), R11 (220Ω, 1/2W), R12 (50Ω, 7.5W), R13 (10K, 1/2W), R14 (10K, 1/2W), R15 (1.2K, 10W), R16 (1K), R17 (10K, 1/2W), R18 (10K, 1/2W), R19 (10K, 1/2W), R20 (10K, 1/2W), R21 (10K, 1/2W), R22 (10K, 1/2W), R23 (10K, 1/2W), R24 (10K, 1/2W), R25 (270Ω, 2W), R26 (4.3K), R27 (270Ω, 2W), R28 (200Ω), R29 (200Ω), R30 (39Ω, 1/2W), R31 (470Ω), R32 (39Ω, 1/2W), R33 (6.2K), R34 (1K), R35 (200Ω), R36 (10K, 1/2W), R37 (10K, 1/2W). Capacitors include C1 (100nF, 50V), C2 (100nF, 50V), C3 (100nF, 50V), C4 (100nF, 50V), C5 (100nF, 50V), C6 (100nF, 50V), C7 (100nF, 50V), C8 (100nF, 50V), C9 (100nF, 50V), C10 (100nF, 50V), C11 (100nF, 50V), C12 (100nF, 50V), C13 (100nF, 50V), C14 (100nF, 50V), C15 (100nF, 50V), C16 (100nF, 50V), C17 (100nF, 50V).

Output Stage: This section drives the speaker. It uses a 2N2222A NPN transistor (Q3) and a 2N2222A PNP transistor (Q4). The circuit is powered by a 15V supply and a 5V DRIVER. Key components include resistors R1 (100Ω), R2 (100Ω), R3 (100Ω), R4 (1K), R5 (100Ω), R6 (200Ω), R7 (200Ω), R8 (1K), R9 (3.3K, 2W), R10 (500Ω, 25W), R11 (220Ω, 1/2W), R12 (50Ω, 7.5W), R13 (10K, 1/2W), R14 (10K, 1/2W), R15 (1.2K, 10W), R16 (1K), R17 (10K, 1/2W), R18 (10K, 1/2W), R19 (10K, 1/2W), R20 (10K, 1/2W), R21 (10K, 1/2W), R22 (10K, 1/2W), R23 (10K, 1/2W), R24 (10K, 1/2W), R25 (270Ω, 2W), R26 (4.3K), R27 (270Ω, 2W), R28 (200Ω), R29 (200Ω), R30 (39Ω, 1/2W), R31 (470Ω), R32 (39Ω, 1/2W), R33 (6.2K), R34 (1K), R35 (200Ω), R36 (10K, 1/2W), R37 (10K, 1/2W). Capacitors include C1 (100nF, 50V), C2 (100nF, 50V), C3 (100nF, 50V), C4 (100nF, 50V), C5 (100nF, 50V), C6 (100nF, 50V), C7 (100nF, 50V), C8 (100nF, 50V), C9 (100nF, 50V), C10 (100nF, 50V), C11 (100nF, 50V), C12 (100nF, 50V), C13 (100nF, 50V), C14 (100nF, 50V), C15 (100nF, 50V), C16 (100nF, 50V), C17 (100nF, 50V).

TESTS:

- 1. X = RF HEAD NUMBER ; X = 4, 5 OR 6
- 2. ALL TRANSISTORS WITH HEAT SINKS (EXCEPT Q5)
- 3. RESISTORS 1/4 W EXCEPT AS NOTED
- 4. R10 800A 25 W DALE TYPE RH-25
- 5. U4 PINOUT IS FOR 8 PIN MIN-DIP PKG ONLY
- 6. KI AMP 5345-1 OPDT RELAY
- 7. ○ DENOTES TERMINAL ON BOARD
- 8. R12 50A 7.5W DALE TYPE RH-5
- 9. C405 IS 19420 NOT USED
- 10. R36 = 47.5K FOR CHANNELS 4 & 5,
511K FOR CHANNEL 6.
- 11. R37 = 59K FOR CHANNEL 4,
61.9K FOR CHANNEL 5,
66.5K FOR CHANNEL 6

Serial	ITEM NO.	QTY	UNIT OR QUANTITY NUMBER	QUANT. USED ON THIS	NOMENCLATURE OR DESCRIPTION	OTHER SIZE	MATERIAL AND/OR MATERIAL SPECIFICATION	WFO CODE	ISSUE REV.
LIST OF MATERIAL									
<div><div><div>UNLESS OTHERWISE SPECIFIED:</div><div>DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS XX = ± .01 XXX = ± .015 ANGULARS ± 1°</div><div>SIN. & TOL. PER ASME Y14.9</div><div>BREAK GRASP DISASSEMBLY ALL SURFACES</div></div><div><div>REORDER</div><div>2/81</div><div>DATE OF ORDER</div><div>DATE</div><div>CROWN</div><div>RATE</div><div>SYSTEM</div><div>DATE</div><div>GROUP</div><div>RATE</div><div>THERMAL</div><div>DATE</div><div>SYSTEM</div><div>RATE</div><div>RF</div><div>DATE</div><div>PERMANENT</div><div>RATE</div><div>ATTACHED</div><div>DATE</div><div>PLEASE:</div><div>REORDER</div><div>DATE</div></div><div><div>THE JOHNS HOPKINS UNIVERSITY</div><div>APPLIED PHYSICS LABORATORY</div><div>JOHNS HOPKINS ROAD, LAUREL, MARYLAND 21112</div><div>SCHEMATIC</div><div>VCO DRIVER TYPE II</div><div>MMG ECM SIMULATOR</div></div></div>									
				888986		D	SK-A-7582	a	
				SCALE		DO NOT SCALE POINT		SHOOT SW	

Figure C-3 — Schematic, VCO driver type II.

signal paths (feedforward/buffer) is flat to within ± 1.5 dB from DC to over 5 MHz. Noise, fill, and other high rate FM signals are coupled to the base of Q2 via C8 and are thus superimposed on the DC tuning voltage present at the output. In this way, approximately 12 V p-p of modulating signal can be added to the DC level of the VCO tuning voltage.

In each RF channel, two VCO's are driven by one VCO driver. Relay K1 is used to connect the driver output to the proper VCO. A second set of contacts on K1 is used to drive the front panel indicator lamps to show which VCO is in use. This relay is driven by U2C and Q5 from the RF relay driver card under control of the HP 9825S.

Figure C-3 shows the schematic of the type II VCO driver. The functional form of this driver is identical to the type I driver, the primary difference being in

the output stage and consequently the output swing which, for the type II driver, is from 0 to -65 V. The ± 5 V signal from the D/A converter is amplified and level shifted by Q1, a PNP transistor operating from a -70 V V_{CC} supply. The noise and fill signals are added through capacitive coupling to the base of Q2 in the same fashion as for the type I driver.

The VCO driver was assembled on two printed circuit cards for the MMG ECM Simulator. One card contains the D/A converter and the high voltage transistor amplifier and buffer. The second card contains the noise and fill input, the auxiliary FM input, and the noise FM buffer amplifier circuit. These cards are mounted in an aluminum chassis which bolts to the main chassis of an RF channel. Figures C-4 and C-5 are pictures of the two cards and Fig. C-6 is a picture of a complete type I driver.

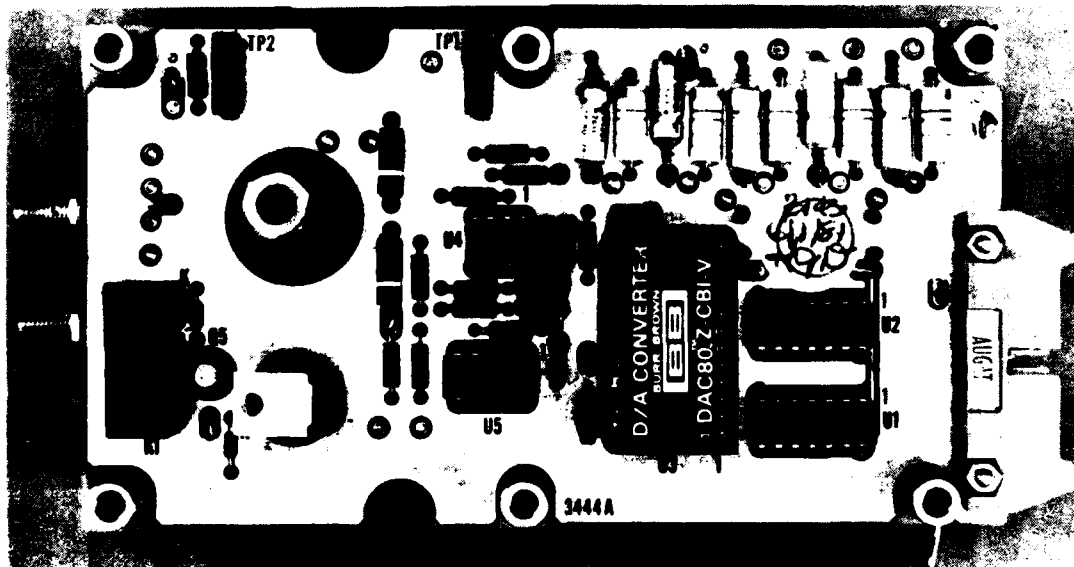


Figure C-4 — D/A converter and high voltage amplifier card.

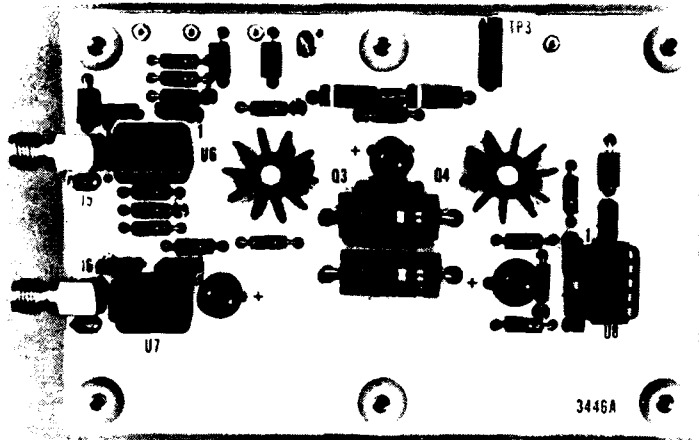


Figure C-5 — Noise buffer card.

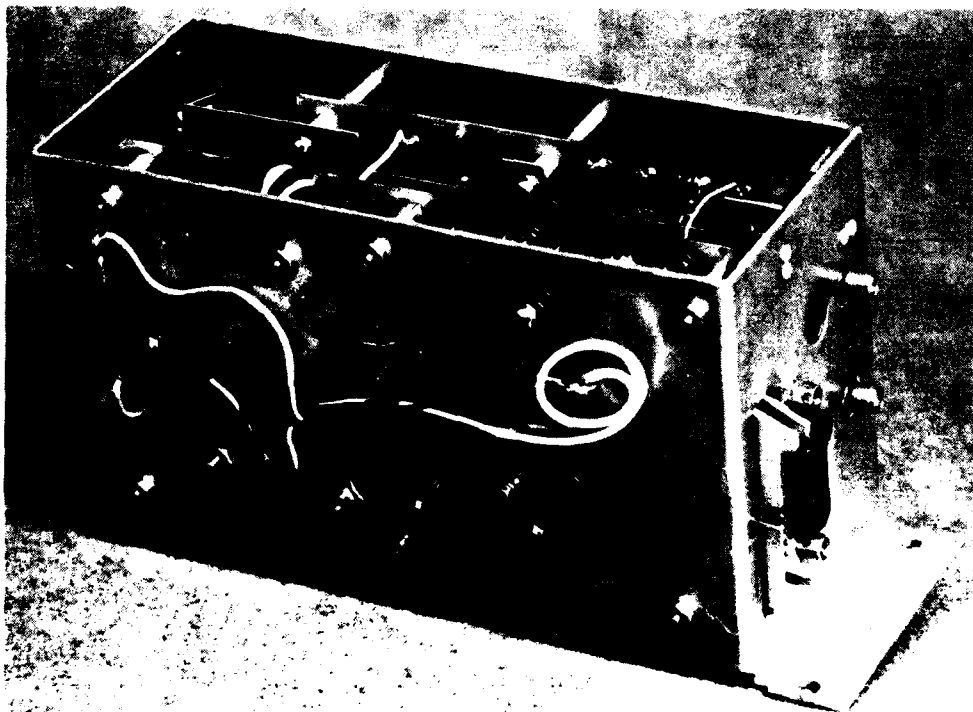


Figure C-6 — Assembled type I VCO driver (cover removed).

APPENDIX D

NOISE FILTER/FILL OSCILLATOR

The MMG Low Frequency ECM Simulator can generate a wide variety of ECM modulation formats under the control of an HP 9825S desktop computer. Two of the modulating signals, Gaussian noise and 100 kHz fill, are processed on the noise filter and fill oscillator card under computer control.

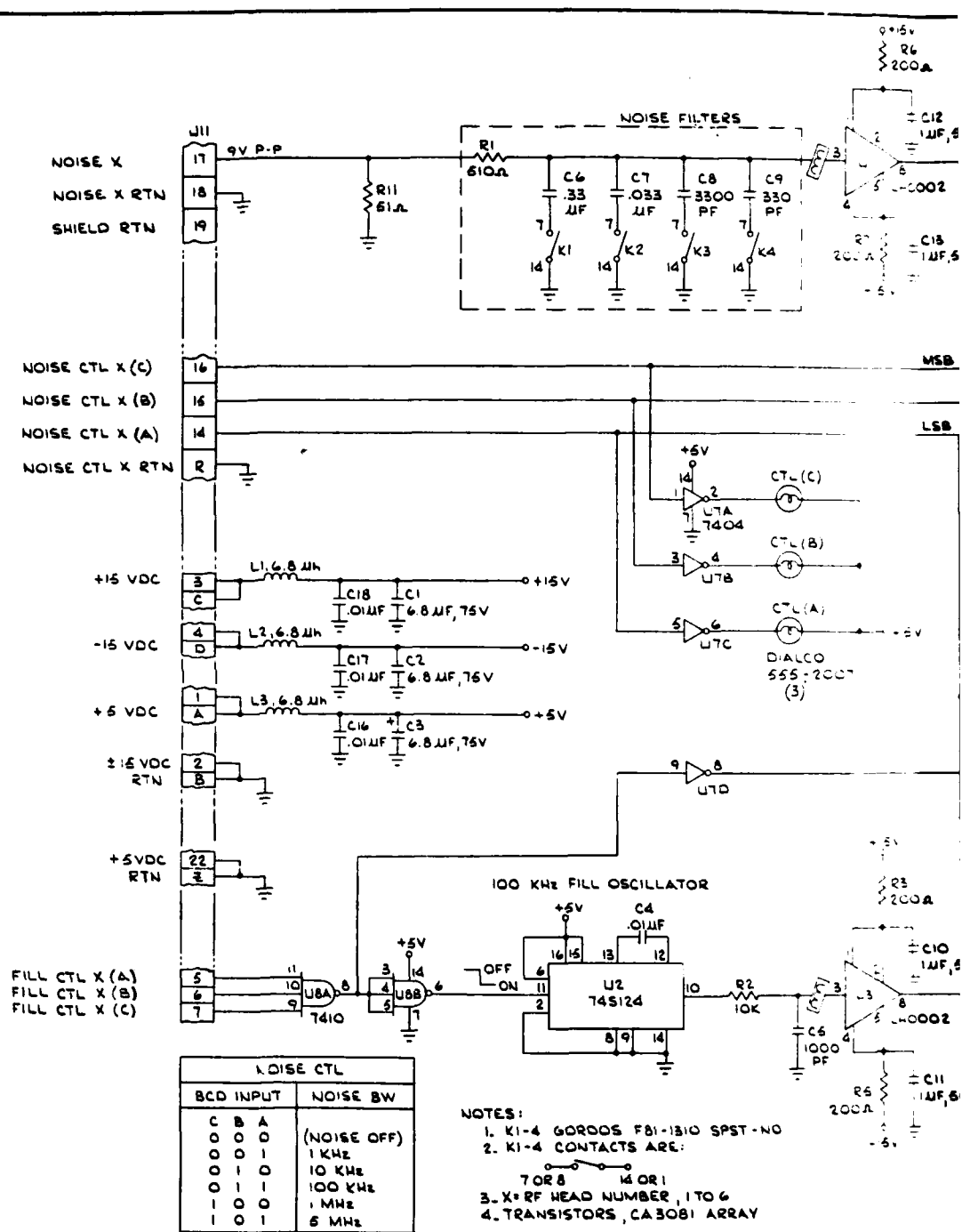
The noise filter and fill oscillator card (Fig. D-1) consists of two separate sections. The fill oscillator section (U8, U2, and U3) generates a 100 kHz triangular waveform that is used to "square up" or broaden the RF spectrum produced by the Gaussian noise modulation. The 74S124 oscillator (U2) will be enabled for all fill oscillator attenuator card codes except 7 (42 dB), and will generate a nominal 100 kHz square wave. This signal is filtered by the low-pass network (R2, and C5) to create the triangular waveshape and coupled to the fill attenuator card via buffer U3.

The remainder of the card is the noise filter circuitry. This portion allows an operator to turn the 10 MHz bandwidth Gaussian noise generator on or off and also to filter the noise through one of four low-pass filter networks. This produces Gaussian noise with bandwidths of 5 MHz (no filtering, full system bandwidth), 1 MHz, 100 kHz, 10 kHz, and 1 kHz, which are selectable under computer control. These filters are selected by closing a relay (K1-K4) that is actuated by binary-to-decimal decoder U4 and drivers U5 and U6.

For example, consider the 1 MHz bandwidth filter. To select this filter, K4 must be closed. The appropriate binary code to accomplish this is 4. If a binary 4 is presented to the three card edge lines (CTL C, B, and A), this will cause the 4 output of U4 (7442) to assume a low state, which will force the output of U5E high and will bias transistor U6E on, thus energizing (closing) K4. Other filters are selected in the same fashion by the use of their respective codes. An exception is code 0, which energizes an off-board relay in the same manner as the others, except that in this case the selected relay contacts are opened, removing power to the noise source module. This is a single-pole, double-throw relay; the normally closed contact pair is used in this application.

Indicators are provided both on and off this card for debugging purposes. The three inverters U7A, B, and C will cause the illumination of the light-emitting diodes associated with any of the control lines that are in a high (TTL logic 1) state. The second binary to decimal decoder U9 (7442) is used in parallel with U4 to provide a front panel indication of the state of the filter card, and one inverter (U7D) provides an on/off indication for the fill oscillator. These signals drive the front panel indicators, which allow an operator to visually monitor the state of the system. The front panel indicators operate in a negative logic sense where a low state on the output indicates that a function has been selected.

Figure D-2 is a photograph of this card.



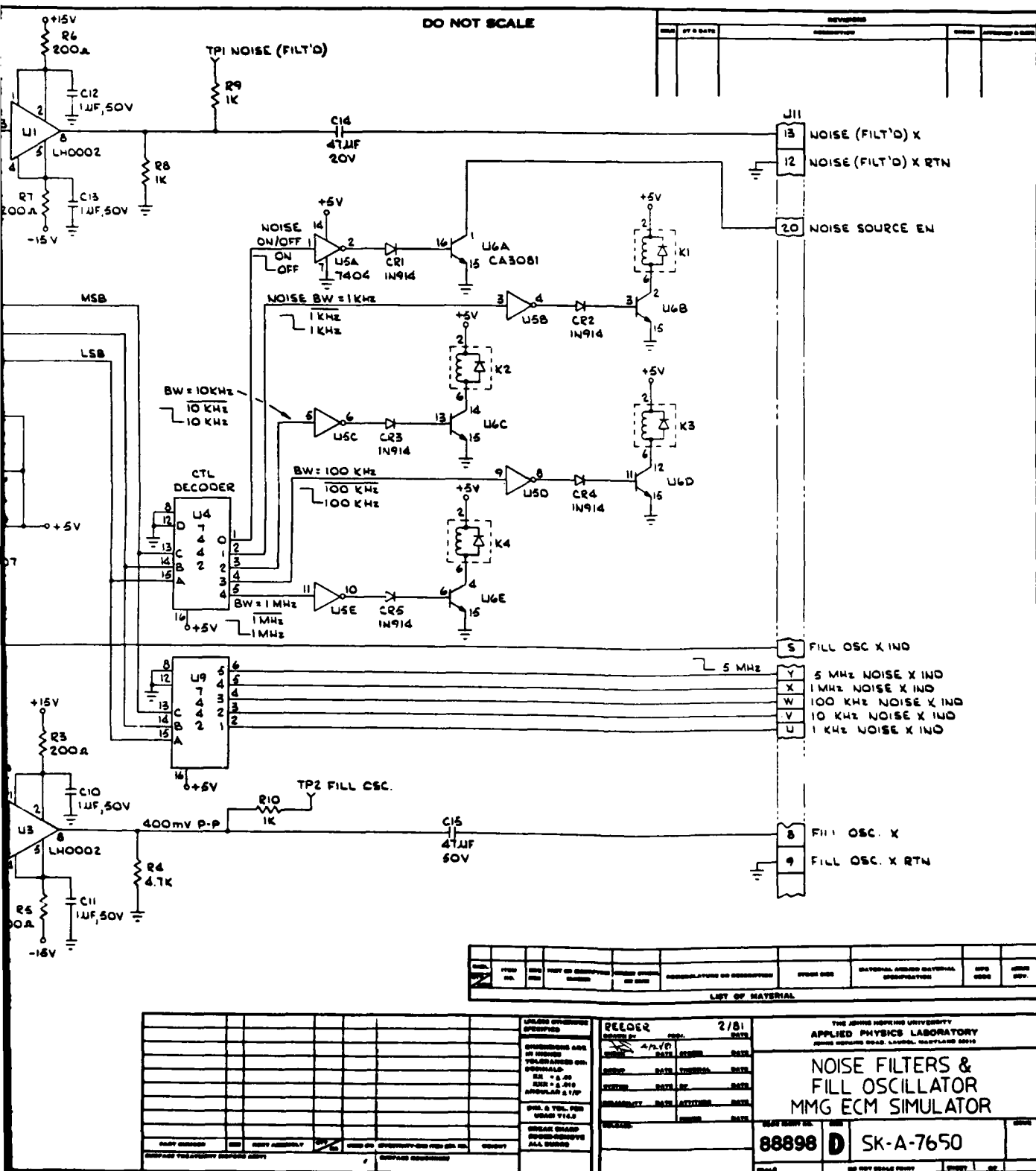


Figure D-1 — Noise filters and fill oscillator.

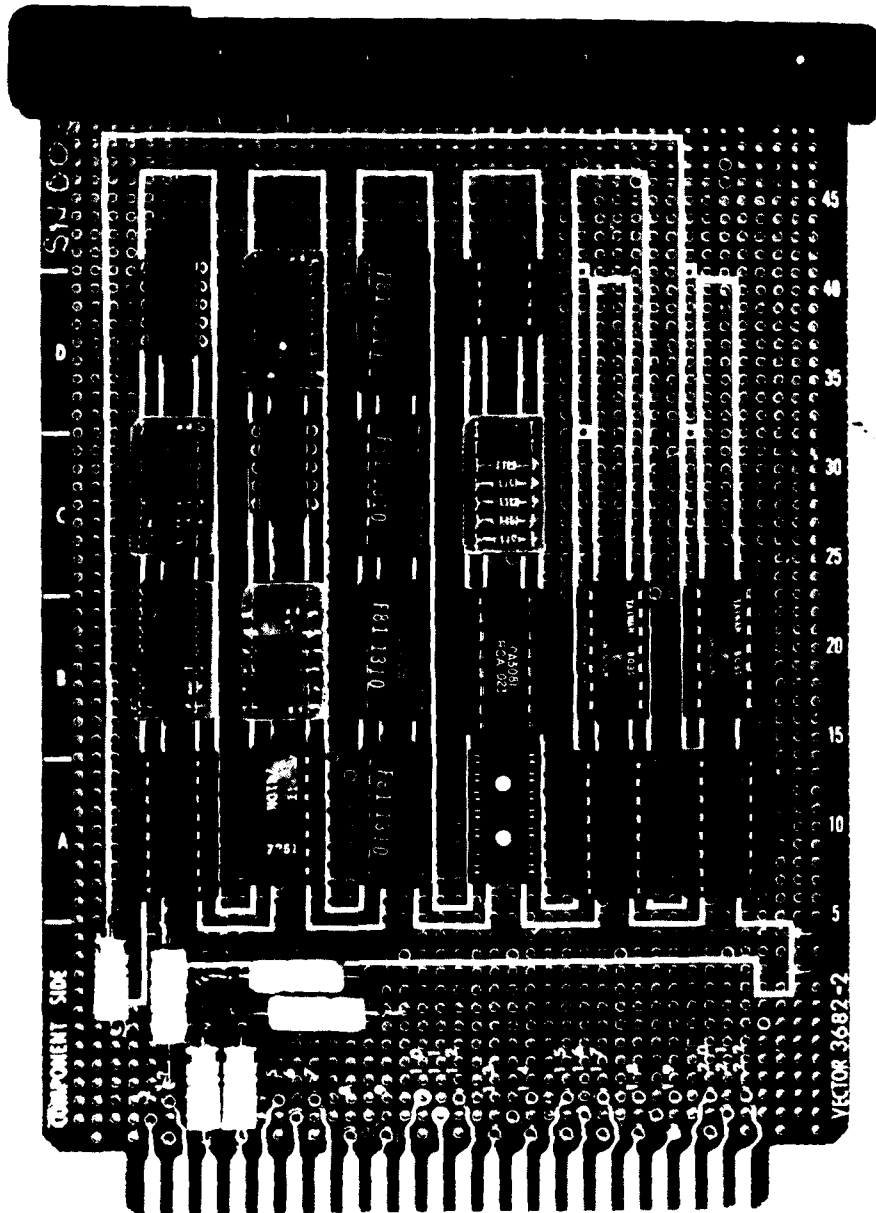


Figure D-2 — Noise filter/oscillator card.

APPENDIX E

NOISE AND FILL ATTENUATORS

The MMG Low Frequency ECM Simulator can generate a wide variety of ECM modulation formats under the control of an HP 9825S desktop computer. Two of the modulating signals used, Gaussian noise and 100 kHz fill, require computer-controlled attenuators for independent control of their amplitude and the RF bandwidth produced. The fill and noise attenuator cards provide a computer-controllable attenuator with a range of 42 dB in 6 dB steps. Three binary lines are required to control each attenuator card.

The attenuator (see Figs. E-1 and E-2) consists of a three section pi-type resistive attenuator with 50 Ω impedance. The sections have individual attenuations of 24, 12, and 6 dB and are selectable independently to provide the full range of 0 to 42 dB in 6 dB steps. A buffer (U1) at the attenuator output eliminates any impedance-related loading problems for the driven circuitry.

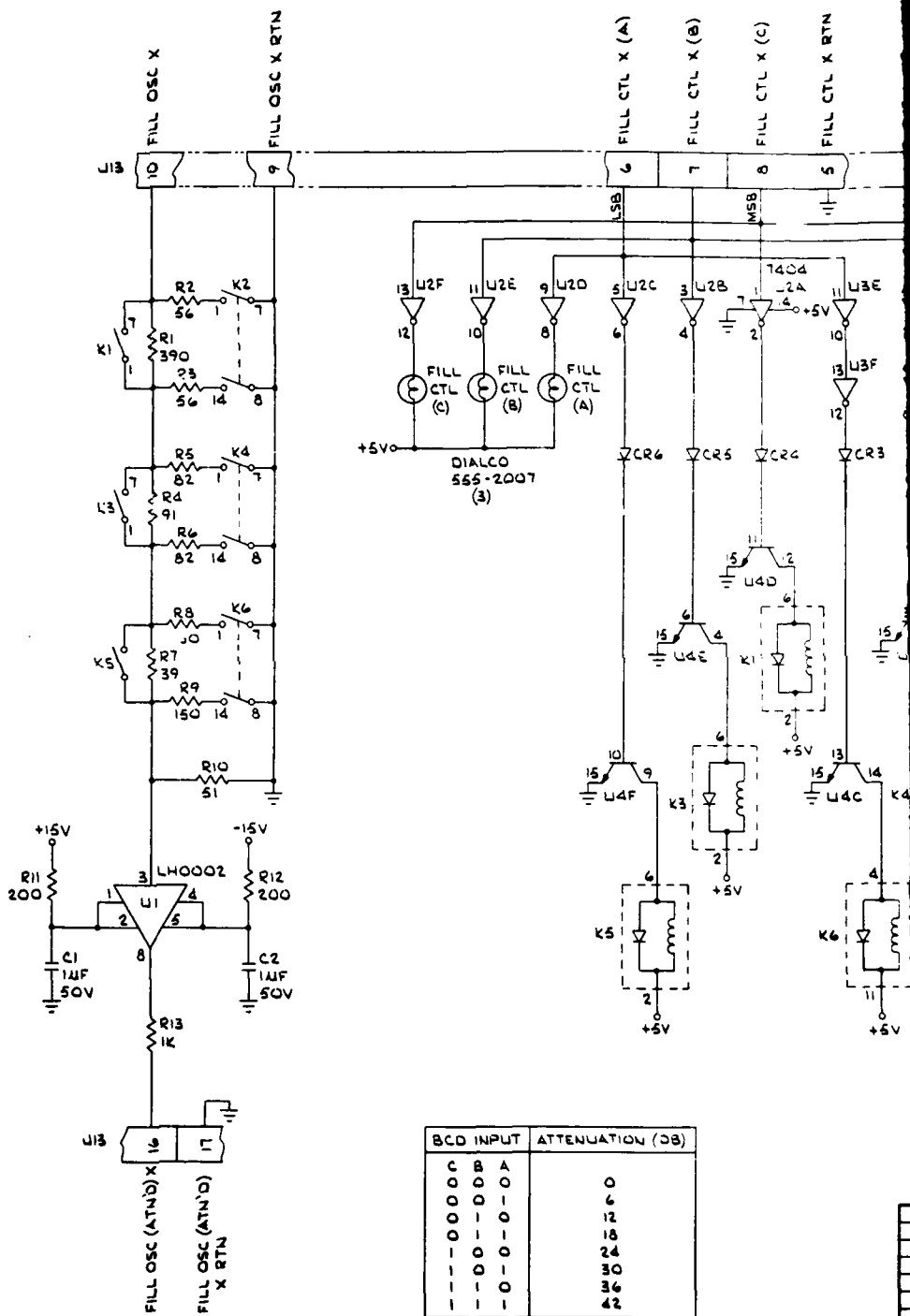
The operation of the attenuator is identical for each section. Consider the section K1, K2, R1, R2, and R3. To select this 24 dB attenuator and place it in the signal path, K1 must be open and K2 closed. This

is accomplished by setting card edge connector pin 8 to a high (TTL logic 1) state. In this condition, the output of inverter U2A will be low, transistor U4D will be off, and K1 will be de-energized and thus open. Similarly the output of U3B will be high and will provide base current to turn on transistor U4A. This energizes K2, thus closing the two contacts shown. To provide an indication of card status for testing, inverter U2F will assume a low output state, which will illuminate the LED associated with the control line. A logic 0 on pin 8 will bypass this attenuator section (i.e., K1 closed and K2 open).

All the other attenuator sections operate in exactly the same way. The code of 0 to 7 to the card edge via the HP 6942A multiprogrammer selects the values of attenuation in 6 dB increments.

The fill attenuator and noise attenuator cards are identical. These cards may be substituted or interchanged if required.

Figure E-3 is a photograph of an attenuator card.



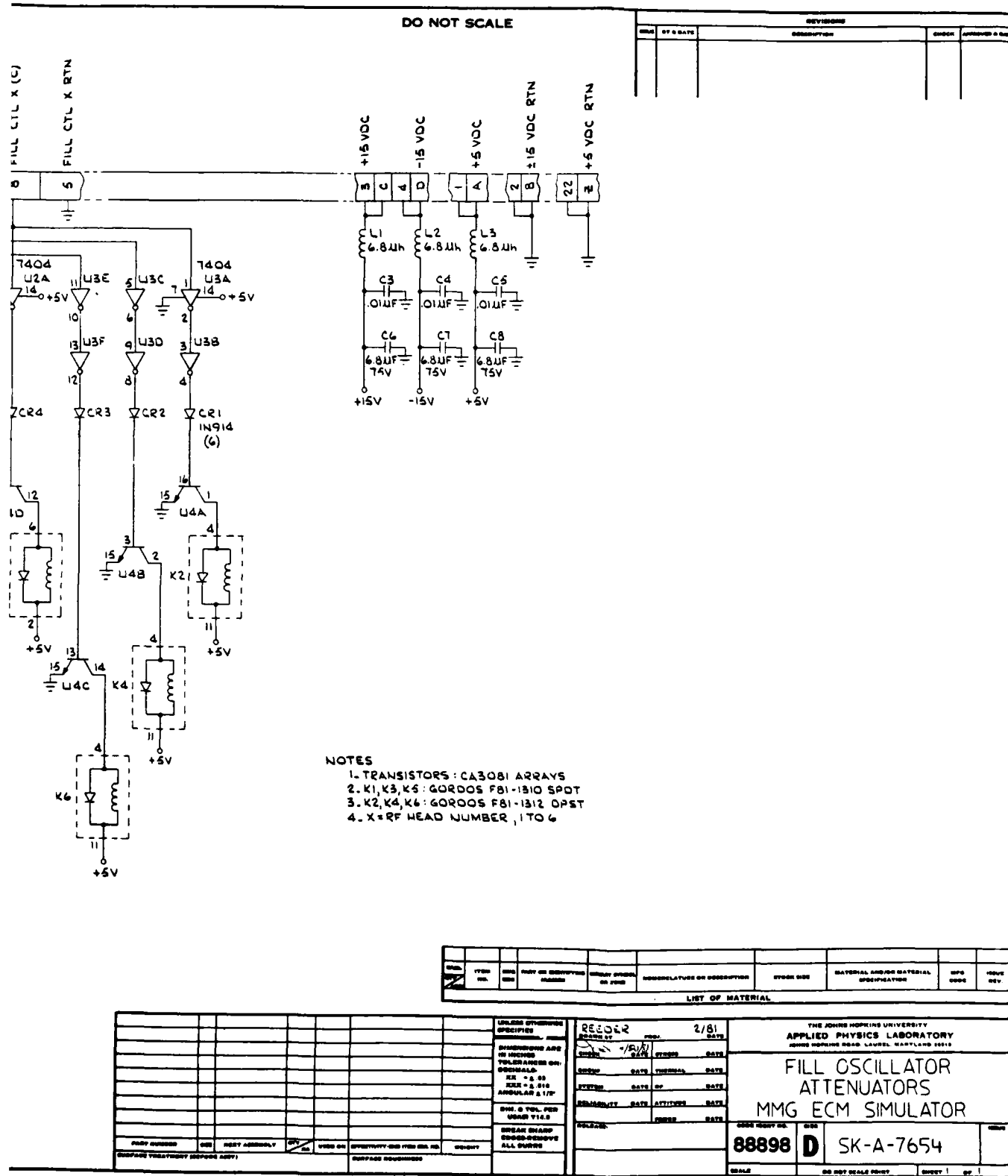


Figure E-1 — Fill oscillator attenuators.

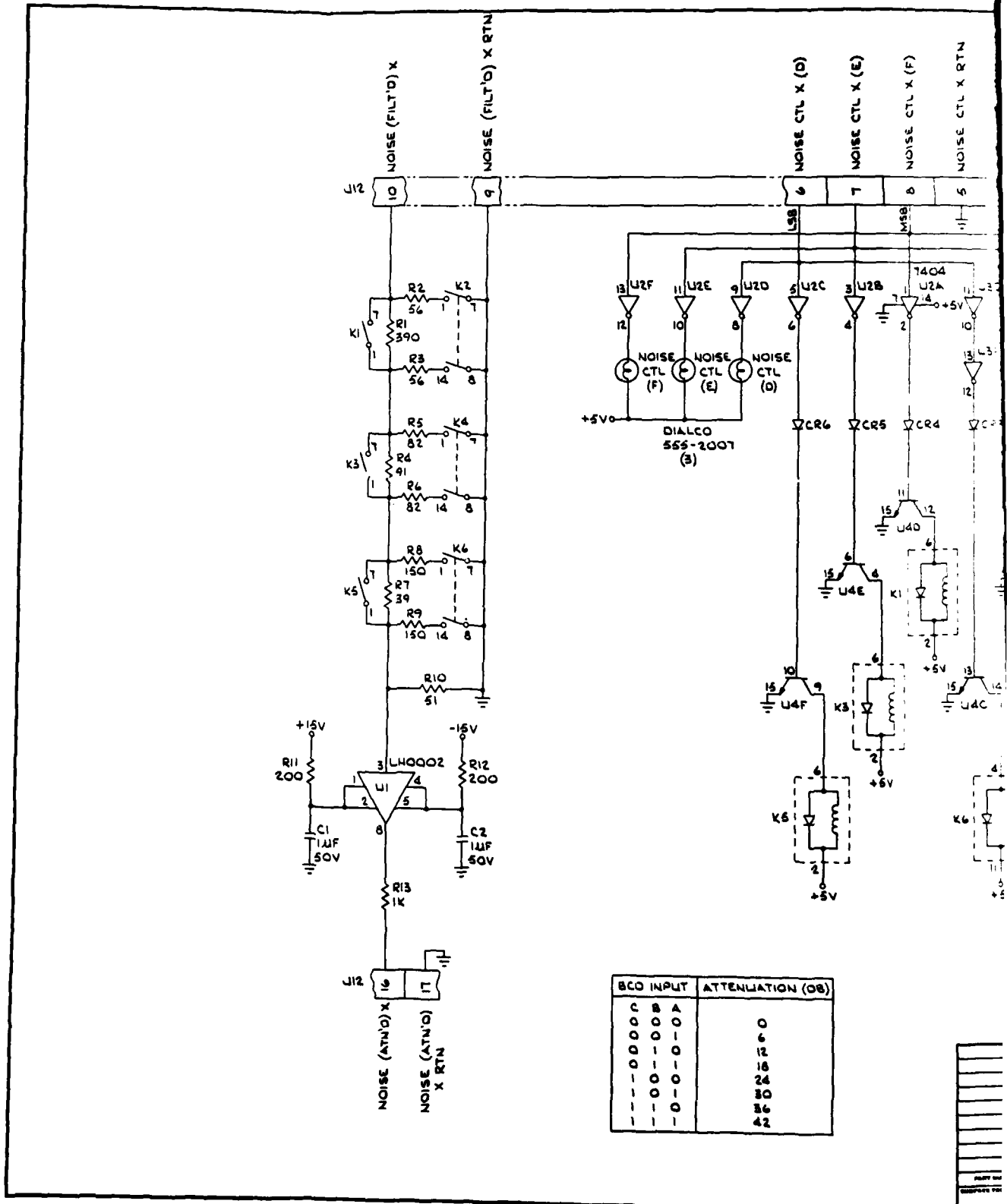






Figure E-3 — Noise/fill attenuator card.

APPENDIX F

RF RELAY DRIVER

This Appendix will describe the driver circuit for the HP 8761A coaxial SPDT VCO relay.

The schematic of the RF Relay Driver card is shown in Fig. F-1. The input to this drive circuit is the VCO (X) SELECT on PIN Y on connector J15. This is buffered by U1 and a noise filter (R13 and C3) before being applied to the inputs of monostable multivibrators U2 and U3. This is the only one of the 16 RF channel control signals that depends upon a transition to cause a control state change. All other control functions operate on static logic states.

The HP 8761A RF relay is a SPDT coaxial relay that is used to connect the selected VCO to the RF modulator circuitry in the RF channel. This relay requires a 12 VDC coil voltage to operate and the state of the relay is switched by reversing the polarity of the coil voltage. The coil contacts are magnetically latching, so that no energy is required to hold the relay in a given state (a pulsed coil drive may be used to reduce power consumption).

In this system, the relay is connected between points B and A (pins S and P of J15) in the transistor array Q1 to Q4. This circuit will reverse the polarity of the coil drive voltage pulse depending on the transitions of the VCO (X) SELECT line. In the quiescent state (no transition) there is no voltage drop across the coil and therefore no power dissipation.

Assume that the VCO (X) SELECT line is making a transition from a low to high (L→H) state (select VCO - A). The sequence of circuit operation is described below:

1. The inputs to monostable multivibrators U2 and U3 will see the transition L→H and the Q1 output of U2 will produce a negative-going pulse (H→L→H). The Q2 output of U3 will not change and will remain low.

2. The output of U5 will follow that of U2 (H→L→H) while the output of U4 will stay low.

3. Pin 3 of U4 is low, so pin 2 of U6A is high; Q5 will be turned on and Q1 will be turned off because its base is low. The output of U6F will be low and Q4 will be turned off.

4. During the low state of the negative pulse at pin 3 of U5 (H→L→H), the output of U6B will be high and Q2 will be turned on. The output of U6D will be low, Q6 will be turned off (emitter H), the base Q3 will be high, and Q3 will be turned on.

5. The following states now exist during the low portion of the H→L→H transition of Q1 of U2: Q1 and Q4 are off, Q2 is on, and Q3 is on with its base at about a 15 V level.

6. Current will flow through R9 and Q3 out of pin S and through the relay coil. The voltage at pin S will be approximately 12 V because Q3 will be operating as an emitter-follower stage with its base at about 15 V. The current return path is through pin P and to ground through Q2.

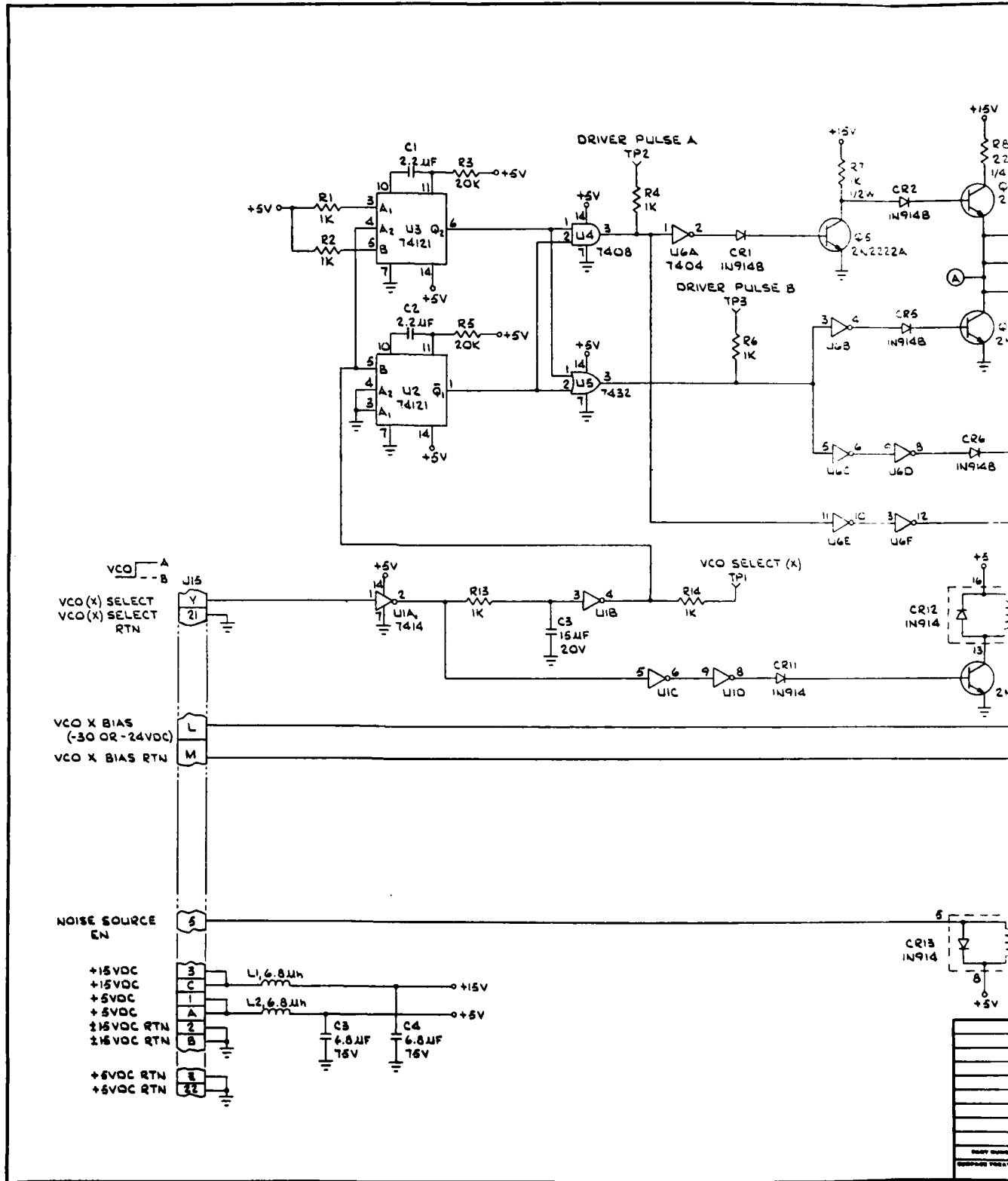
7. When the H→L→H transition on pin 3 of U5 is completed, pin 3 will be high and Q3 and Q2 will be off, so that no current will flow in the relay coil.

The H→L transition of the VCO SELECT line will create a L→H→L transition at pin 6 of U3. This will cause current to flow in the opposite direction by turning on Q1 and Q4 while keeping Q3 and Q2 in the off state.

Diodes CR7, CR8, CR9, and CR10 are transient-suppression diodes across the relay coil. The 1N4746A zener diode conducts when the voltage across it exceeds 18 V. The diode assembly shown is required because the voltage polarity across points A and B will reverse when the relay is made to change state.

Transistors Q5 and Q6 are used as voltage amplifiers to drive the bases of Q1 and Q3, respectively. Transistors Q1 and Q3 operate as emitter followers.

Figure F-2 is a photograph of this card.



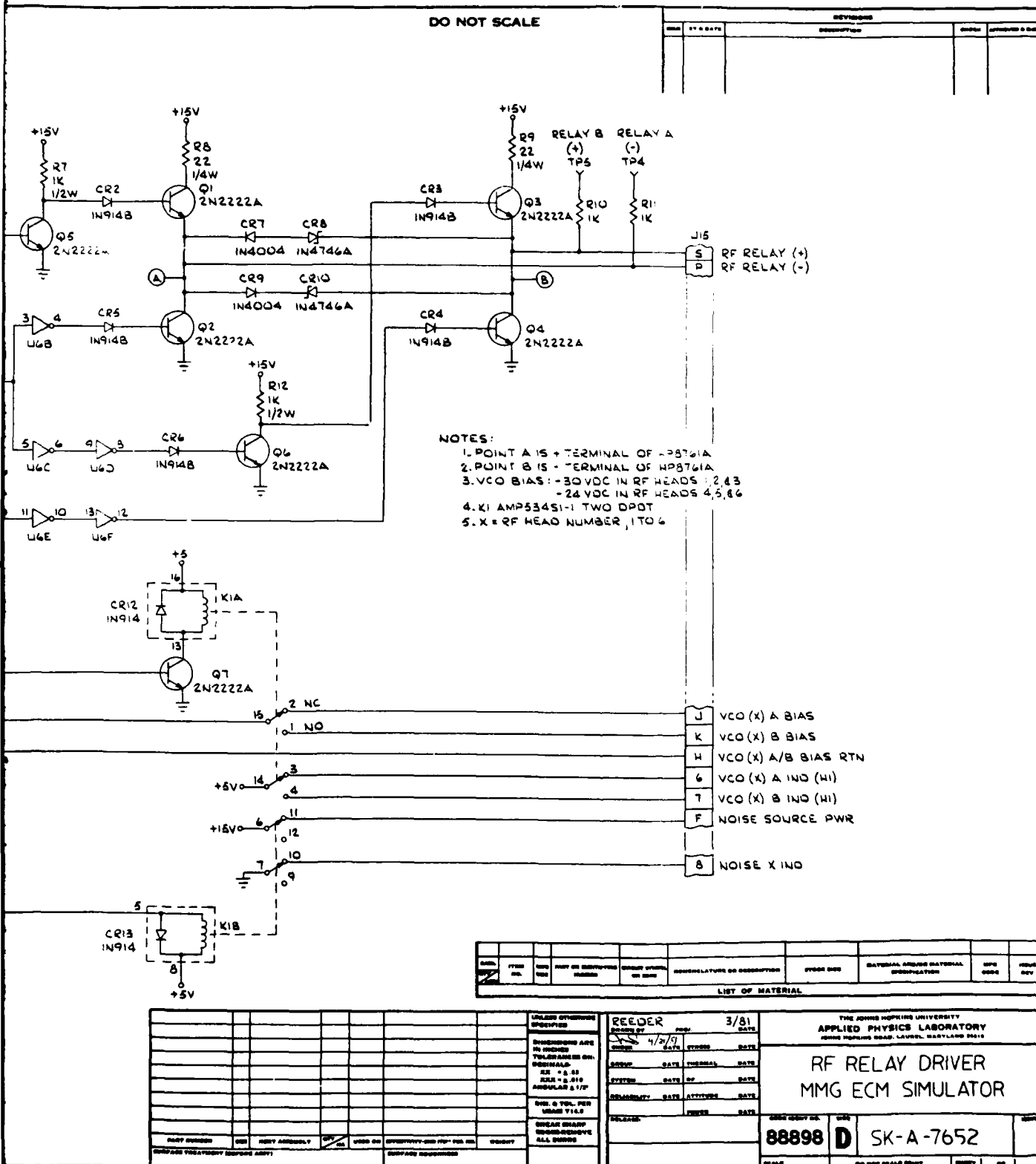


Figure F-1 — RF relay driver.

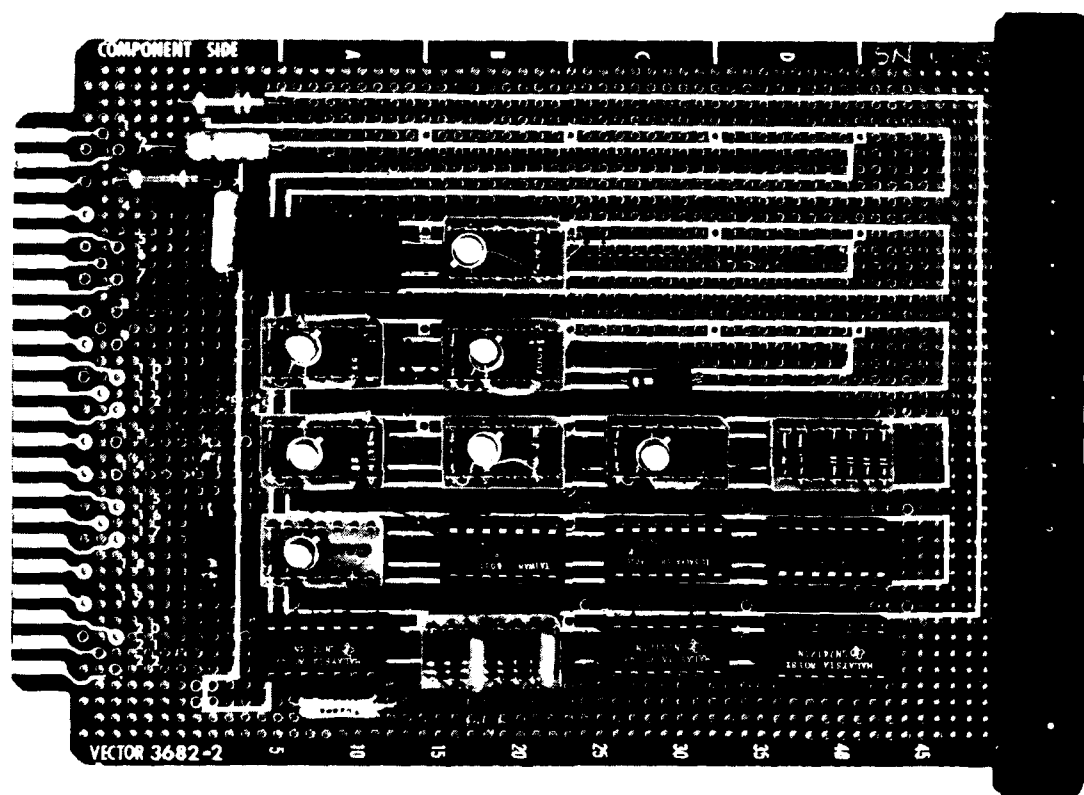


Figure F-2 — RF relay driver card.

APPENDIX G

BIPHASE MODULATION DRIVER

The biphas modulation driver provides a bipolar current drive of ± 50 mA to the double-balanced mixer in the RF channel to pass the RF signal either with its phase unchanged or shifted by 180° . This two-state phase modulation generates either comb or noiselike RF spectra for ECM testing.

Three BCD control lines (labeled biphas CTL A, B, and C) are used to control the state of the driver. An operator may select either RF carrier on or off (approximately 30 dB attenuation), a comb spectrum, or a pseudorandom noise spectrum. The tooth spacing of the RF comb may be set at 5, 10, or 20 MHz; the mainlobe bandwidth of the $[(\sin x)/x]^2$ shaped noise spectrum may be 10, 20, or 40 MHz. The driver is controlled by the HP 9825S computer through the HP 6942 multiprogrammer.

Figure G-1 is the schematic of the biphas modulation driver.

The clock frequency is set by control lines A and B (CTLX(A) and CTLX(B)). If both these lines are high, U1 (a voltage-controlled oscillator) will be disabled and no clock signal will be generated. The clock is disabled to reduce spurious noise pickup when the biphas modulator mixer is turned on. The 74S124 is enabled and generates a 20 MHz square wave for all other states of the control lines. This 20 MHz clock is divided by U2A and U2B to produce the 10 MHz and 5 MHz clocks. The 4:1 multiplexer U4 selects the clock signal to be used. An external TTL clock may be used if required by selecting the 5 MHz clock via the HP 9825S, removing the rear panel coaxial jumper, (J17 to J18) and connecting the clock signal to the external oscillator input (J18). The external clock frequency should not exceed 20 MHz.

The pseudorandom sequence generator is composed of U5, U6, U7, U8, and U10, forming a 28 cell linear feedback shift register. The signals from taps placed at cells 3 and 28 are modulo 2 added by U10 and fed back to the input to generate a maximal length pseudorandom sequence. The sequence will repeat every $(2^8 - 1)$ clock cycles. The "delayed start" circuit (formed by U3 and C15) preloads the shift register with a known nonzero pattern and inhibits shifting for a few milliseconds to allow clock start-up transients to die out. This is needed because excessive jitter in the clock signal could force the

register into its all zero state and effectively stop it.

The pseudorandom sequence and the clock signal are applied to U9A and U9C, respectively. Depending on the state of control line C (CTL X(C)) either the clock signal or the pseudorandom sequence will appear at the output of U9D. If either or both control lines A and B are low, pin 5 of U3B and pin 15 of U13 will be high and the clock signal or the pseudorandom sequence will be routed through the switch U13, and current driver U15 to drive the balanced mixer. Capacitor C2 and the resistor network R7, R4, and R8 allow level-shifting the TTL-level signal so that the bipolar current drive required by the balanced mixer can be generated.

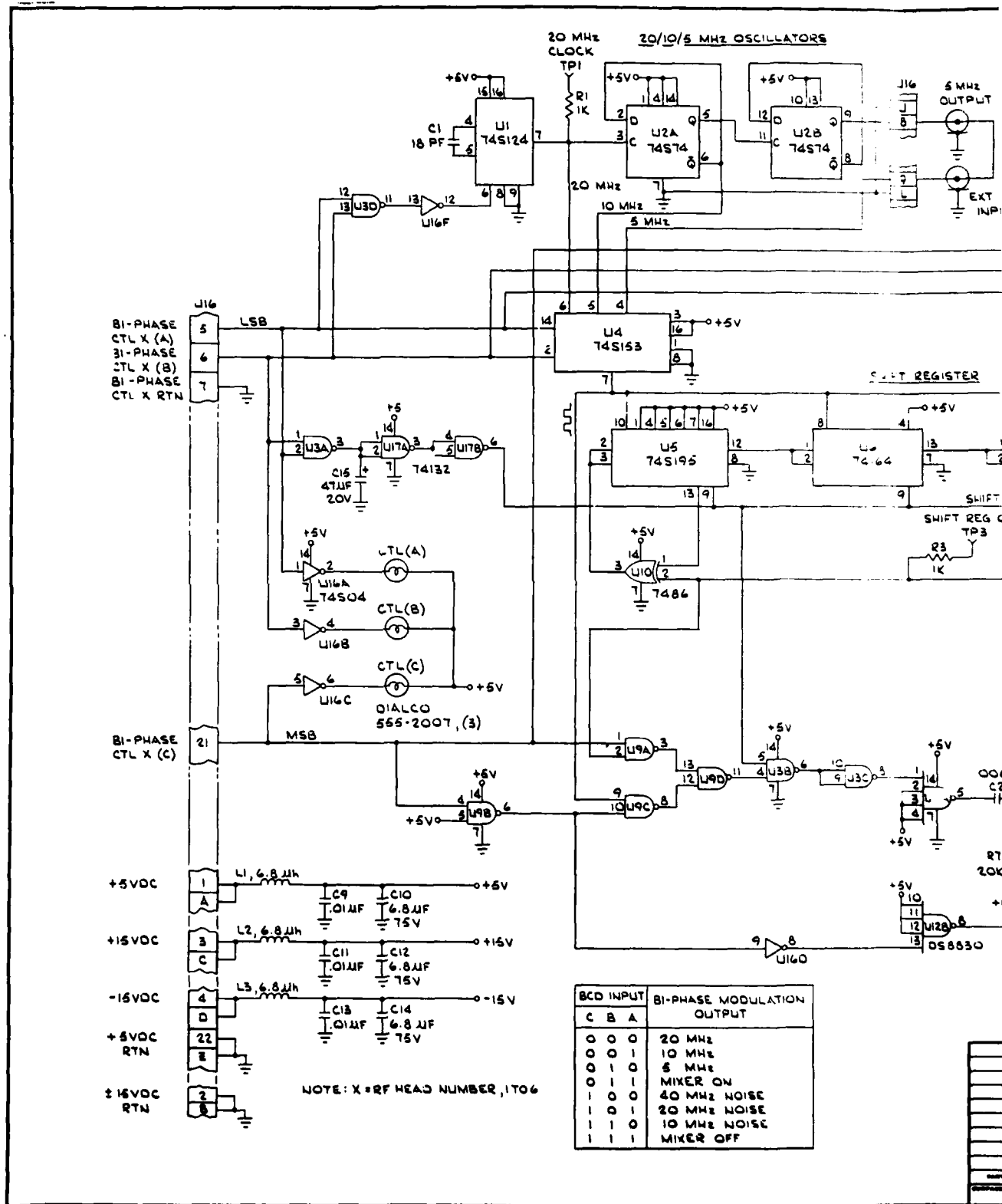
If both control lines A and B are high and the biphas mixer is turned on (CTL C = 0) the output of U12B will be high and an approximately 1 VDC bias level will be applied to input 4 of U13. Pin 15 of U13 will be low so the bias signal will be routed through switch U13 and a positive current will flow through the balanced mixer, allowing the RF carrier signal to pass.

If all control lines are high (mixer off), pin 15 of U13 and the output of U12B will both be low. This will result in a 0 V output from U13 and U16, and no current will flow through the balanced mixer. When the mixer is in its off state it attenuates the RF carrier by approximately 30 dB. In practice this state (BCD code = 7) is of little use. The attenuation is not constant from one RF head to another nor is it constant with frequency. This state may be used along with the "carrier off" state of the pulse modulator if desired, but it should not be used by itself because of the unpredictable level of isolation it provides.

Indicator lights are mounted on the card to allow the operator to monitor the states of the three control lines for debugging purposes. U16 serves as a driver for these LED's.

Decoder U11 provides seven drive signals to the front panel to indicate whether the comb or pseudorandom noise signal has been selected, and the bandwidth of the modulation drive signal. These LED indicators are visible on the front panel photographs.

Figure G-2 is a photograph of the biphas modulation card.



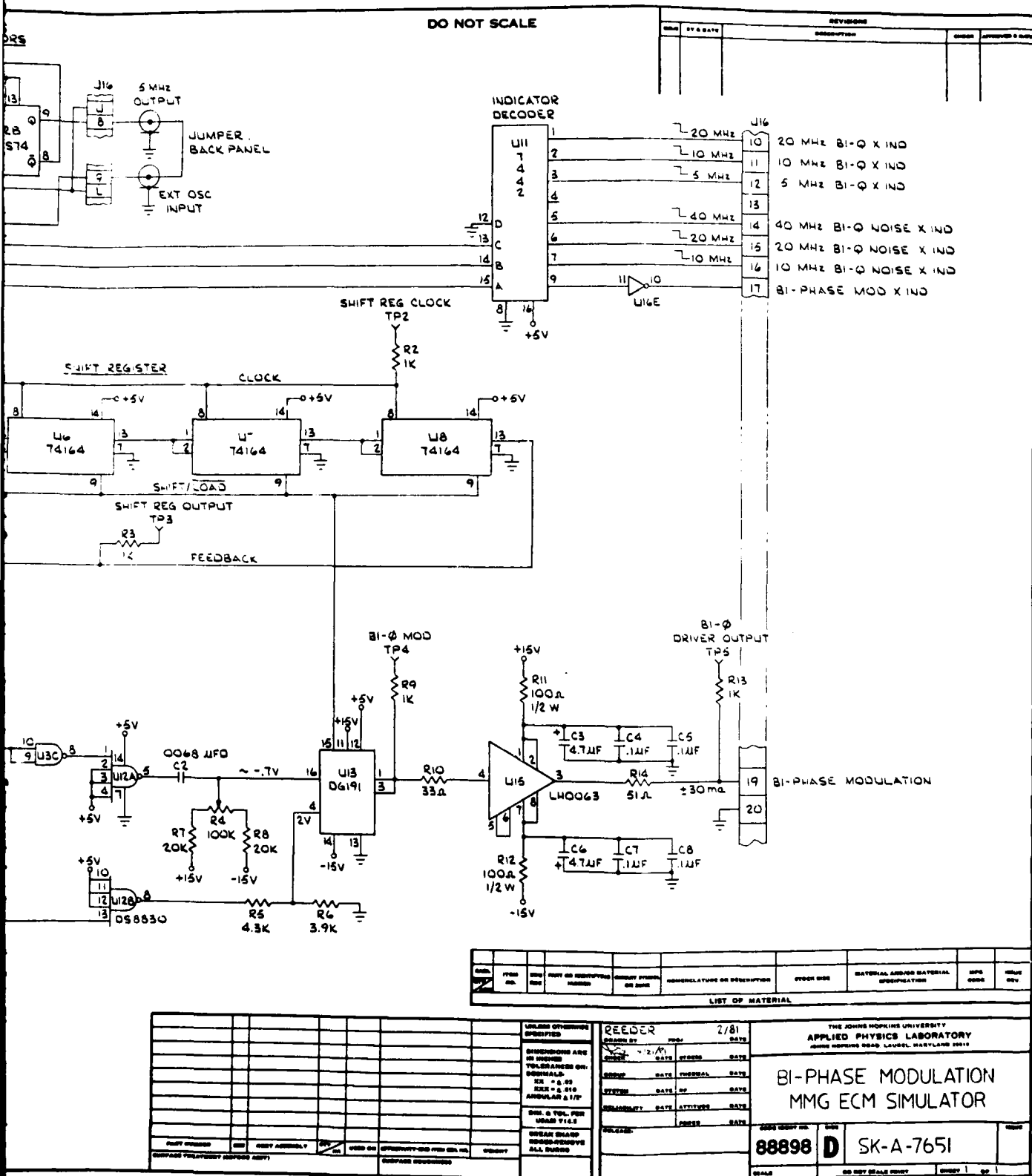


Figure G-1 — Biphase modulator.

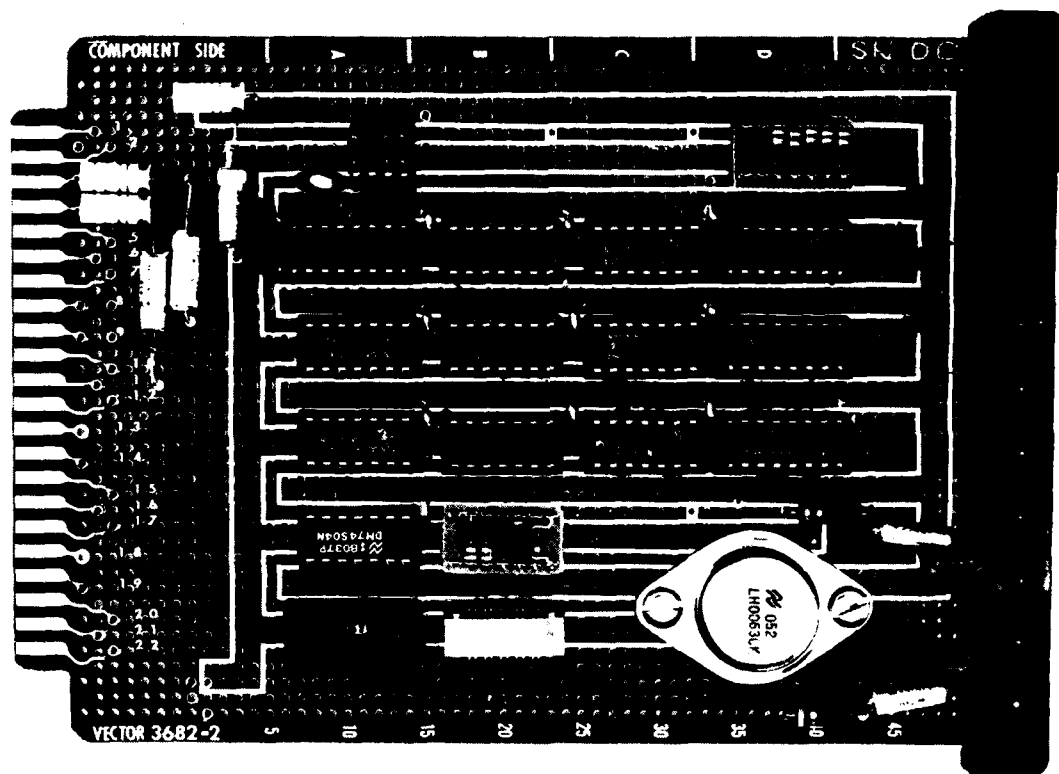


Figure G-2 — Biphas modulator driver card.

APPENDIX H

PULSE MODULATION SELECTOR

The pulse modulation selector card allows an operator to pulse the RF output at arbitrary rates and duty cycles under computer control.

This card drives a PIN diode RF switch with a TTL control signal. This switch has rise and fall times that are typically 155 ns and 700 ns, respectively, and will provide greater than 65 dB of "off" state isolation between the input and output.

The schematic diagram of the pulse modulation selector is shown in Fig. H-1.

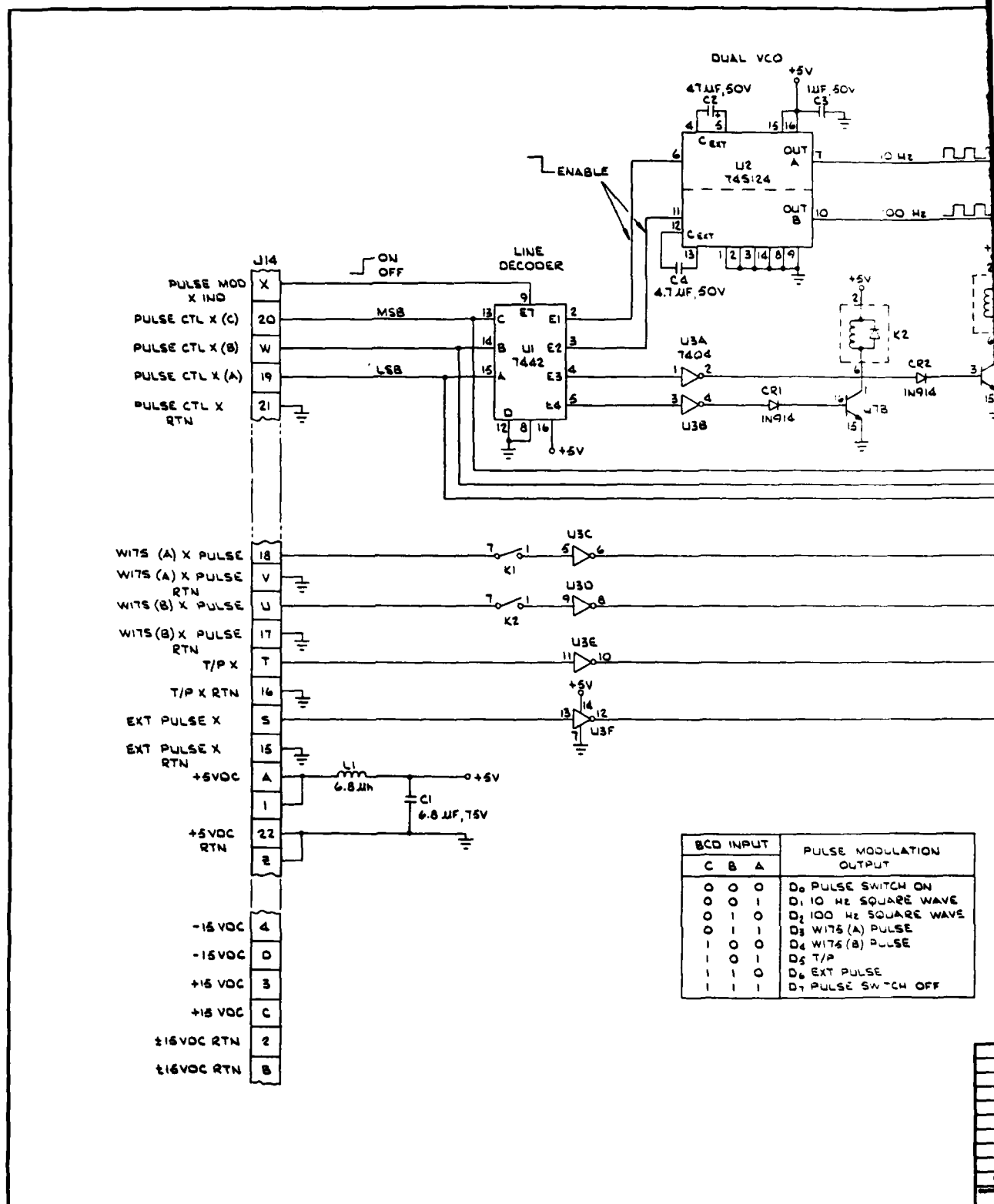
The three BCD control lines allow eight unique inputs to be connected to the RF switch. Data selector U4 (an 8-to-1 multiplexer) connects one of the eight inputs to the PIN diode RF switch as determined by the BCD control word. Decoder U1 is used to select one of the two fixed-frequency internal oscillators (U2) or close one of the two relays (K1 or K2) that isolate the Wavetek 175 arbitrary waveform generators. Decoder U1 is used with decoder U5 to drive the front panel LED indicators that show the status of the pulse modulator circuitry.

The RF output can be turned on or off using this card or it can be blinked by one of six sources:

1. Either a 10 Hz or 100 Hz square wave at a 50% duty cycle.
2. One of two Wavetek 175 arbitrary waveform generators, which can be programmed to create any arbitrary rate or duty cycle.
3. The timer/pacer card in the multiprogrammer, which can be programmed to generate a 50% duty cycle square wave at rates up to 1 MHz.
4. An external pulse generator.

Both front panel and on-card indicator signals are decoded on this card to act as a debugging aid and status indicator for the operator. Inverters U6A-C display the status of the three control lines directly on the card, while U5 decodes the control line code to drive the appropriate front panel indicators. The E7 output of U1 is used to drive the front panel indicator that shows whether or not the pulse modulator circuit has been selected. The LED is illuminated for all codes except 7, to indicate that the pulse modulator switch is in an active state and passing RF energy to the output at a duty cycle ranging from greater than zero to 100%.

Figure H-2 is a photograph of this card.



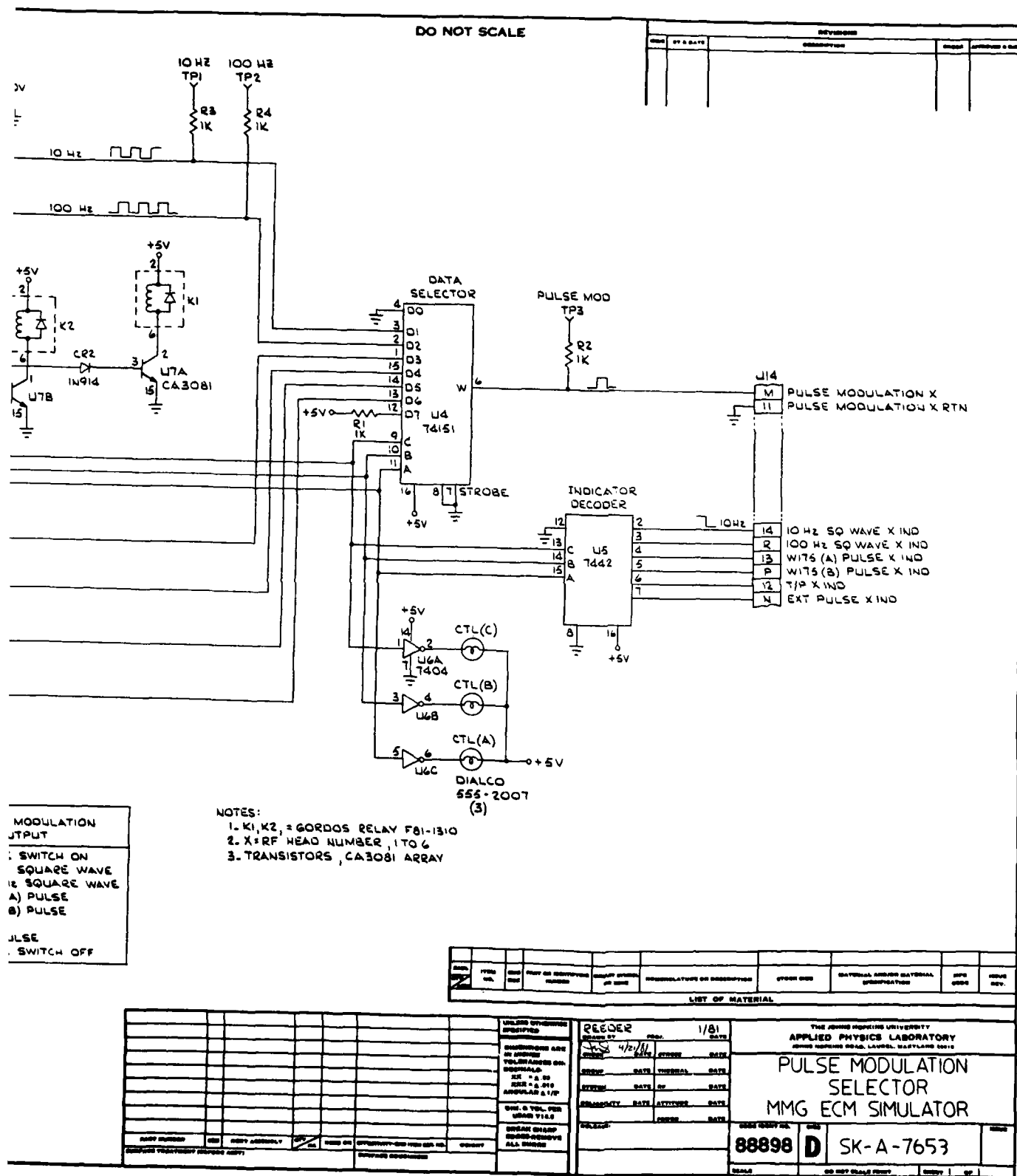
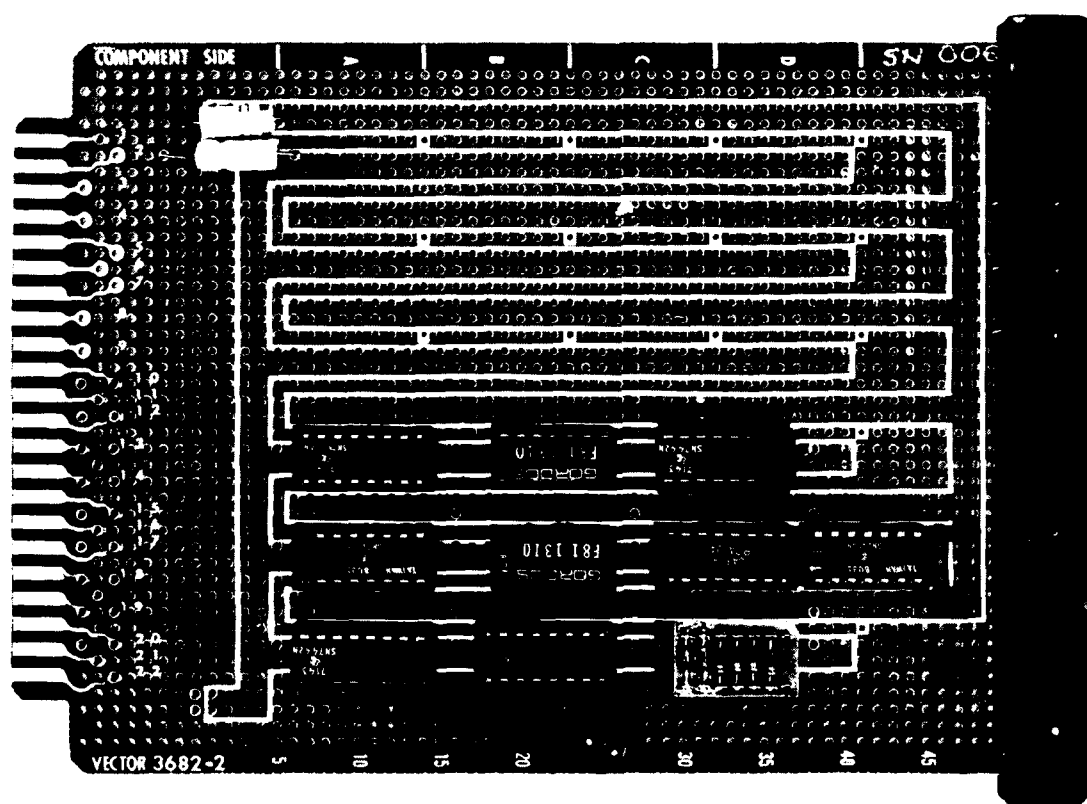


Figure H-1 — Pulse modulation selector.



APPENDIX I

AM AND FM MODULATION SWITCH MATRIXES

The schematics of the AM and FM modulation switch matrixes are shown in Figs. I-1 and I-2. These cards are identical, so that the discussion in this appendix, while referring to Fig. I-1, will apply equally to either the AM or FM switch matrix.

There are five BCD lines that control this matrix. Three (AM HD CTL (A), (B), and (C)) go to decoder U1 to identify the RF channel number. A code of 1 to 6 will address one of the latches U3 to U8, which correspond to RF channels 1 to 6, respectively. For a code of 0 or 7, no latch will be enabled. Capacitors C13 to C18 are required at the outputs of U1 to suppress transients (which could enable the wrong latch circuit).

The other two control lines (AM MOD CTL (D) and (E)) identify the type of auxiliary modulation and go to U2 (a dual 2-line to 4-line decoder). For four input binary codes ($\# = 0$ to 3), the corresponding 1Y# and 2Y# outputs of U2 will be low. These low signals are used as data inputs to the 7475 latches (U3 to U8).

The codes and their modulation sources are:

- 0 – no auxiliary modulation.
- 1 – Wavetek 175 arbitrary waveform generator.
- 2 – D/A card in the HP 6943 multiprogrammer extender.
- 3 – External AM or FM input.

The latch that has been selected by U1 will accept the data input provided by U2 and will close or open the proper relays to route the specified modulation to the selected RF channel. For example, if RF channel code 6 (110) is sent to U1 and modulation code 1 (01) is sent to U2, the latch U8 will be enabled (G input high). The 1Y1 and 2Y1 outputs of U2 will be low and this input at pin 2 of U8 will cause the pin 16 and 1 outputs to assume low and high logic states, respectively. The high logic state on U8, pin 1, will turn on Q16 to close relay K61, which connects the Wavetek

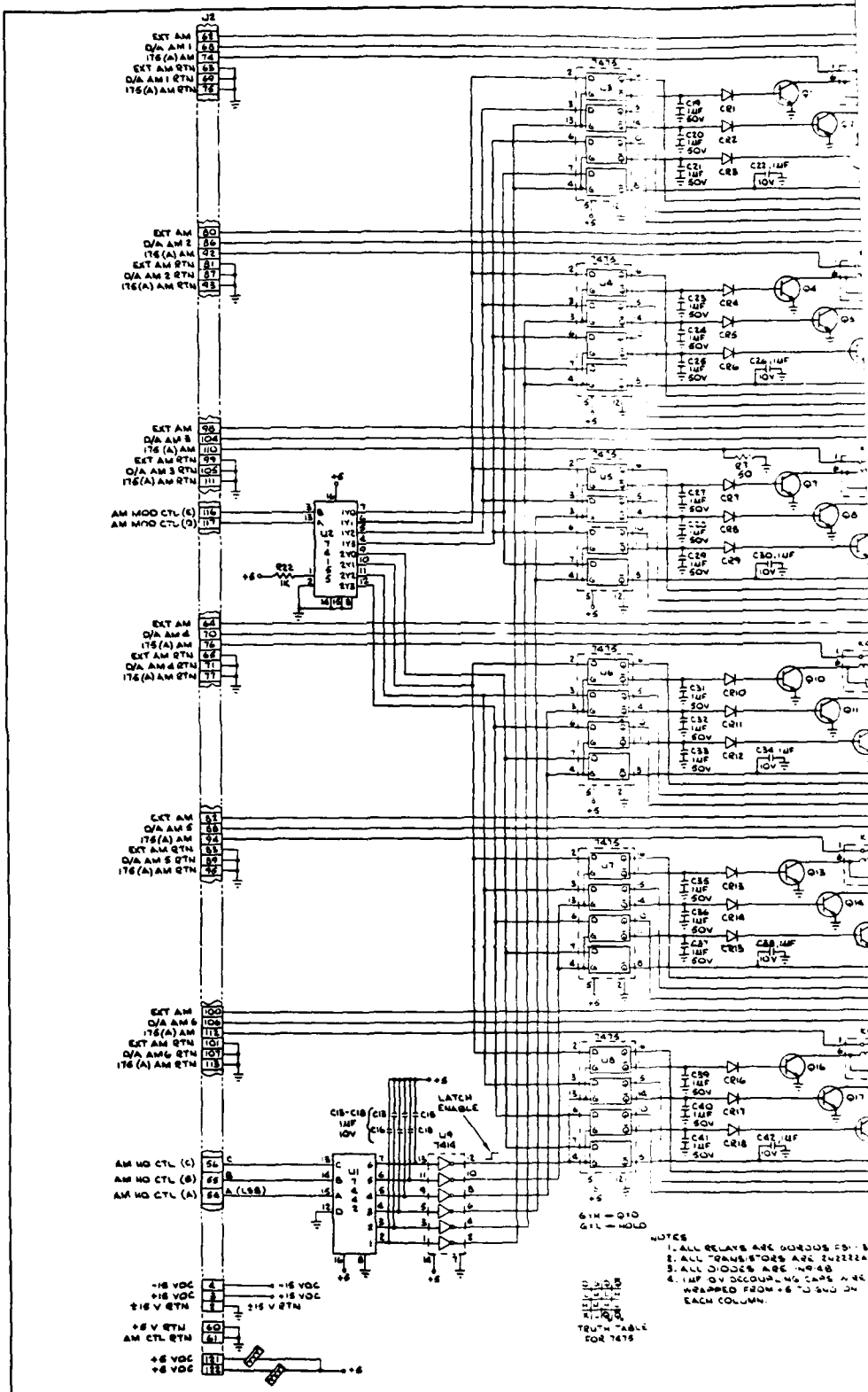
signal source input to the RF channel 6 output through buffer U14. The low logic state on U8, pin 16, will activate a front panel indicator lamp to show that the Wavetek has been selected as a signal source for RF channel 6. The input to U1 and then to U2 may now be changed to address another RF channel. The selected state for RF channel 6 will be held by latch U8 until it is changed. Only a code 0 input to U2 is slightly different. This opens any signal path relay which may have been closed by deselecting all of the three relays associated with the RF channel.

The relay numbering scheme identifies each relay according to its RF channel and modulation code. For example, relay K61 controls the signal path for the code 1 (Wavetek) input to RF channel 6. The numbering scheme is also the same as the row, column illustration used in the description of this card in the body of this report.

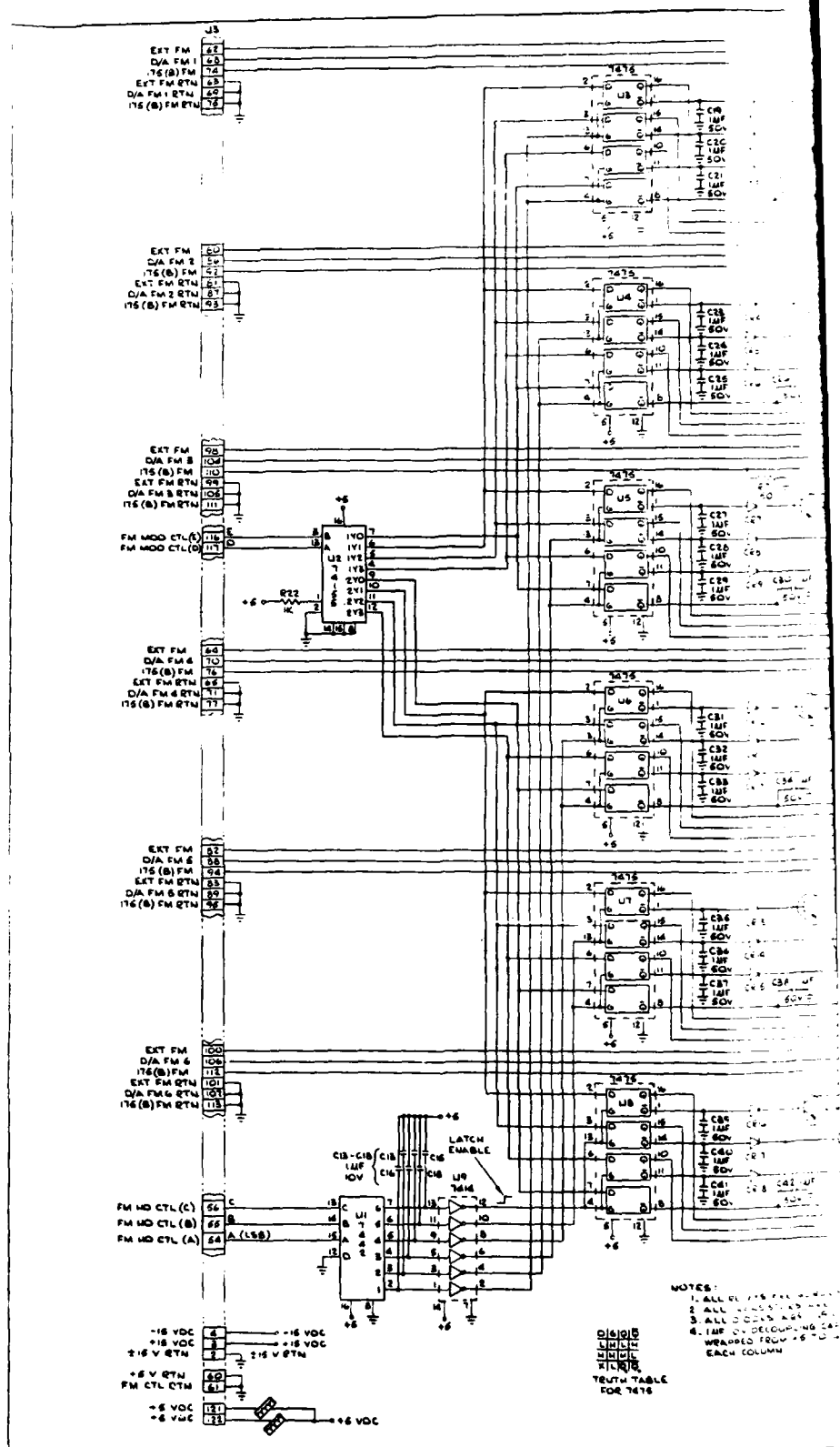
During the design phase, a potential noise problem was discovered that affected the latch states. It was found that if the low output of a 7475 latch in the circuit was momentarily pulsed high, the latch would change state even though the gate line was held low and the latch was disabled. In the relay driver circuit, a low output from the latch is used to keep the signal path relays off. In order to prevent noise or switching transients from falsely changing the state of the latch, capacitors C19 to C42 were added to the latch outputs.

The 3 dB passband of the signal path on the matrix card from input to output is over 5 MHz. This wide bandwidth is required by the auxiliary FM input of the VCO driver circuit. The drivers (U9 to U14) have bandwidths far greater than this and, due to the spurious coupling on the wire-wrap card, could oscillate. The tendency to self-oscillation on this card is suppressed by the RC decoupling networks on the ± 15 V power supply lines of the buffer and also by a ferrite bead on the input lead.

The switch matrix circuit is assembled on an Augat wire-wrap card. Figures I-3 and I-4 are photographs of this card.







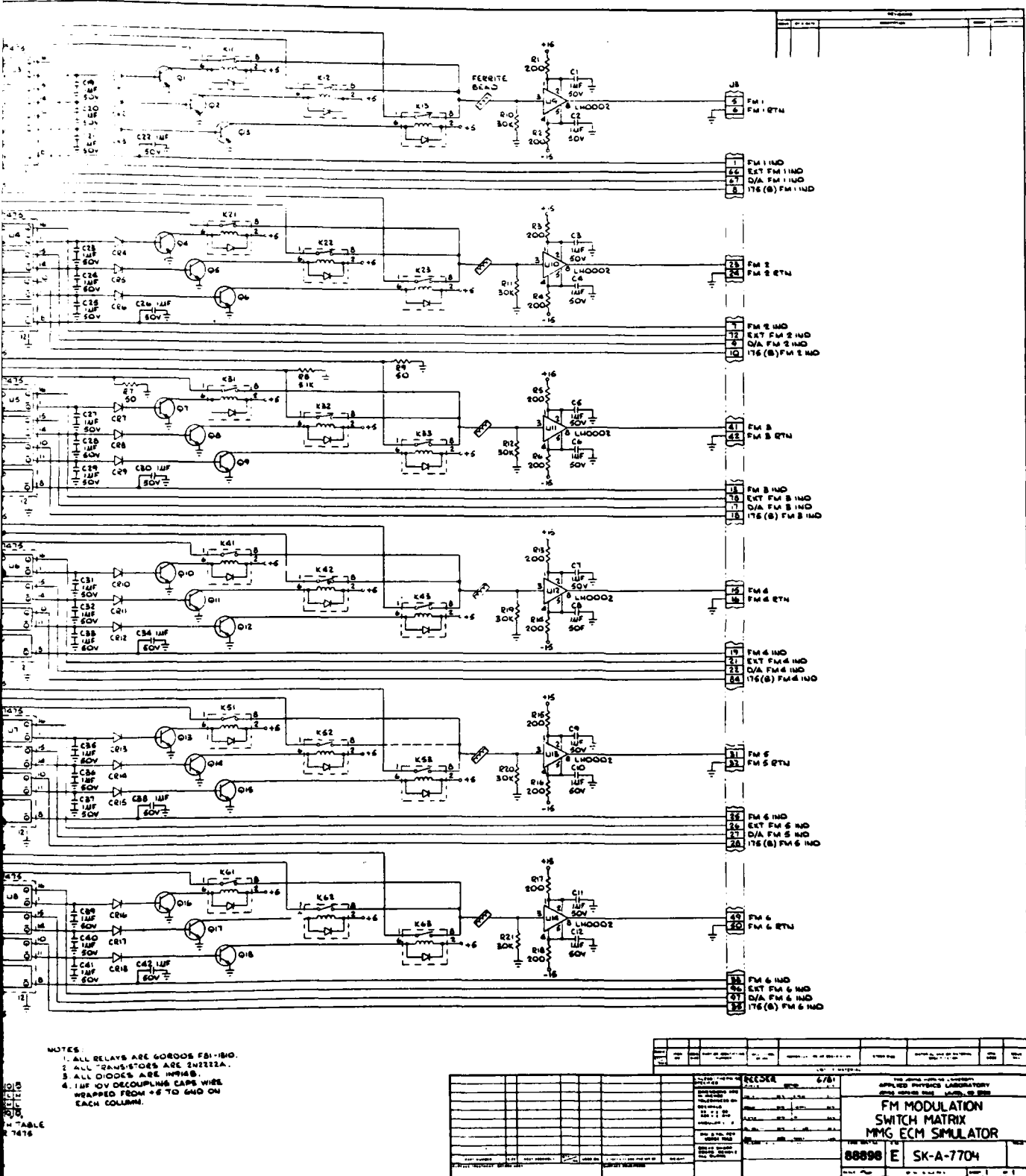


Figure 1-2 — FM modulation switch matrix.

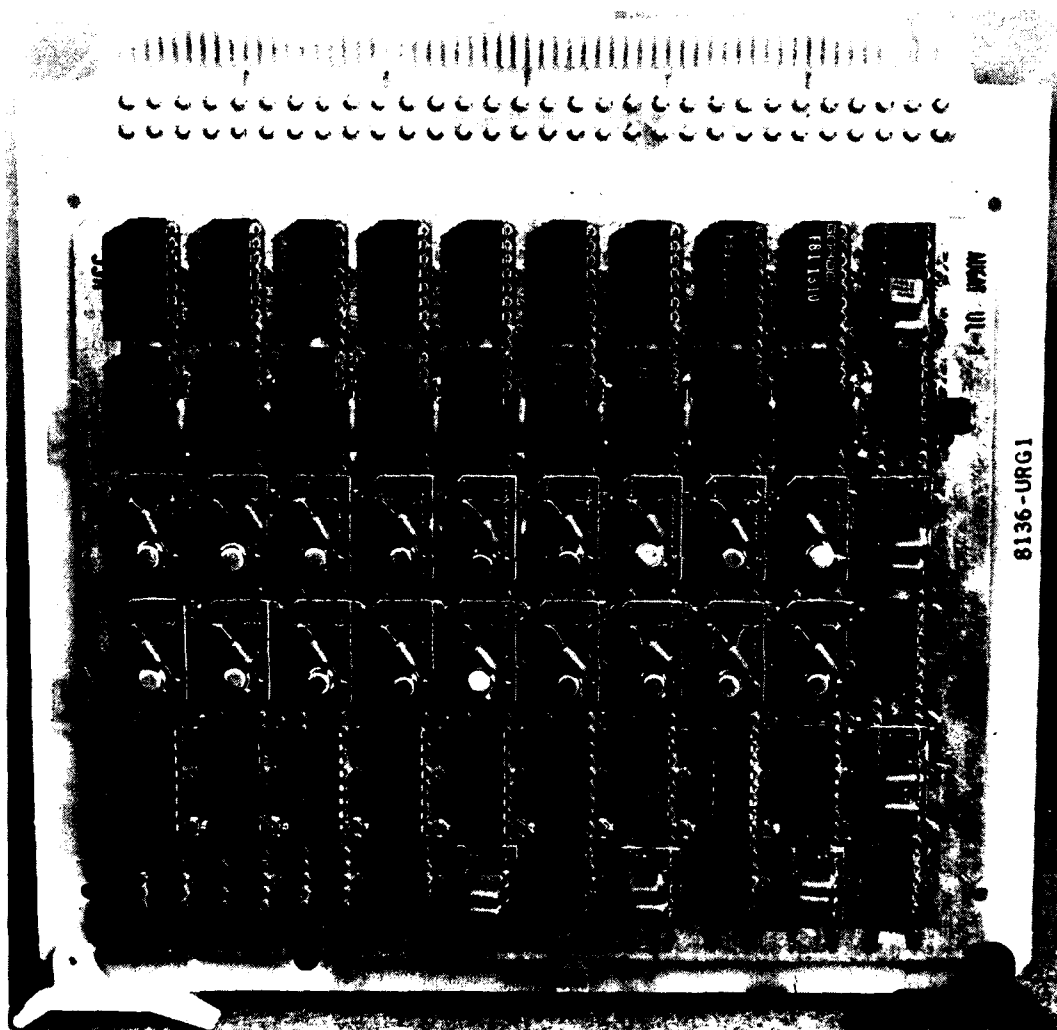


Figure 1-3 — AM/FM modulation switch matrix card.

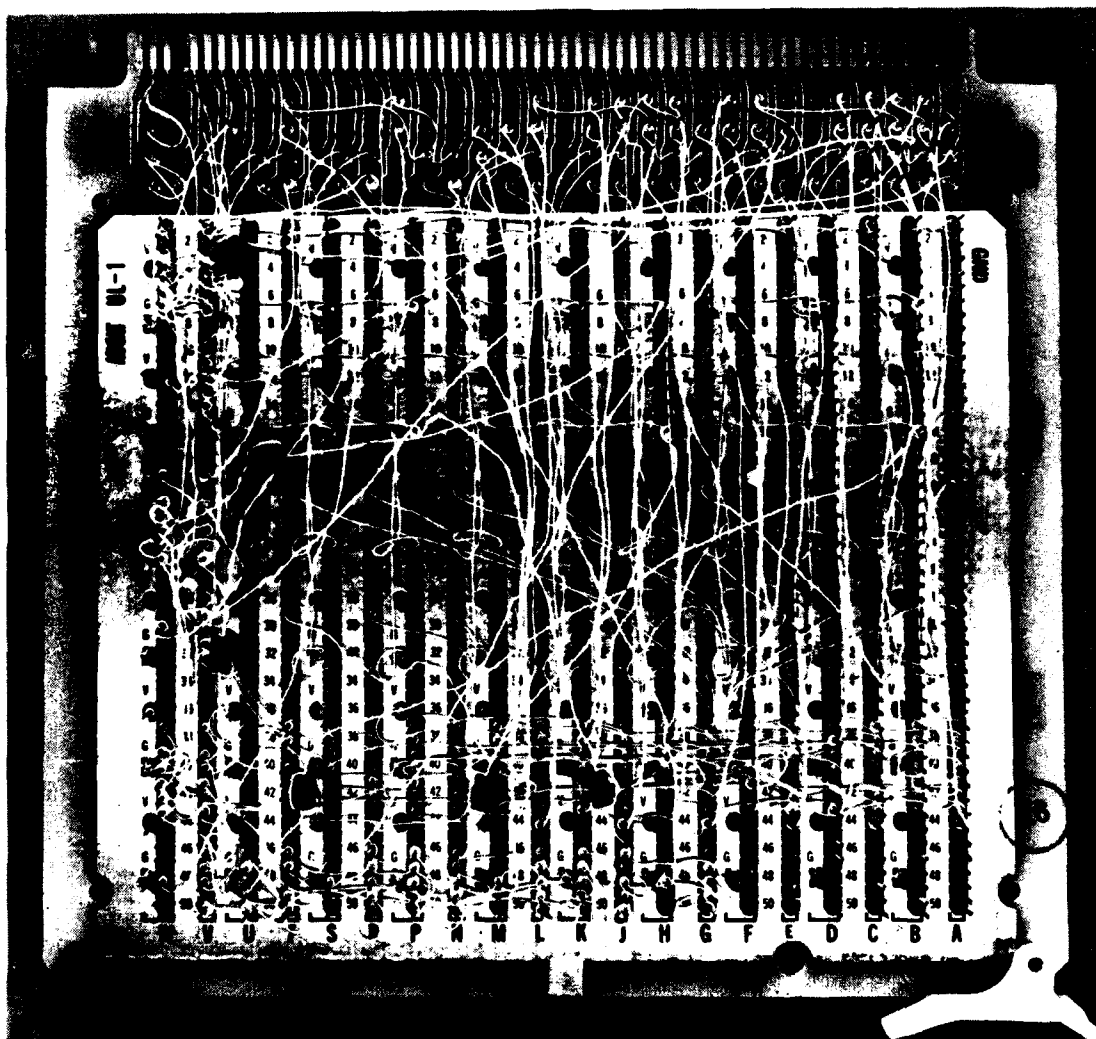


Figure I-4 — AM/FM modulation switch matrix, rear view.

APPENDIX J

LEVEL-SET ATTENUATOR DRIVER

The schematic of the level-set attenuator driver is shown in Fig. J-1. The level-set attenuator driver card consists of six driver circuits. Each driver controls an HP 8494H/8495H attenuator pair in an RF channel.

The two attenuators have seven attenuation sections with values of 1, 2, 4, 4, 10, 20, and 40 dB. Each section has two solenoids that act to either insert or remove the attenuation from the signal path. Therefore each driver section must drive 14 solenoids as shown by the J1-15 to -28 outputs from driver 1 (see Fig. J-1). The attenuator sections are magnetically latching so that once a section is set, it will remain in that state until changed.

The card is controlled by 10 input lines. Seven of these lines represent the attenuation code and three specify the driver to be enabled. The attenuation code control lines are labelled D1 to D7 and correspond to the 1, 2, 4, 4, 10, 20, and 40 dB attenuator sections, respectively. A logic 1 on one of these lines will cause that value of attenuation to be inserted when the driver is enabled and a logic 0 will cause the attenuation to be removed. To minimize power dissipation the solenoids have internal switches that break the solenoid current path after switching has occurred. This means that current will only flow in a solenoid during the 20 ms transition time.

Consider driver 1 as an example. If input D1 is high, pin 2 of F8 will be low and pin 5 of F8 will be high. When a BCD code of 0 is applied to S1-3 the Y0

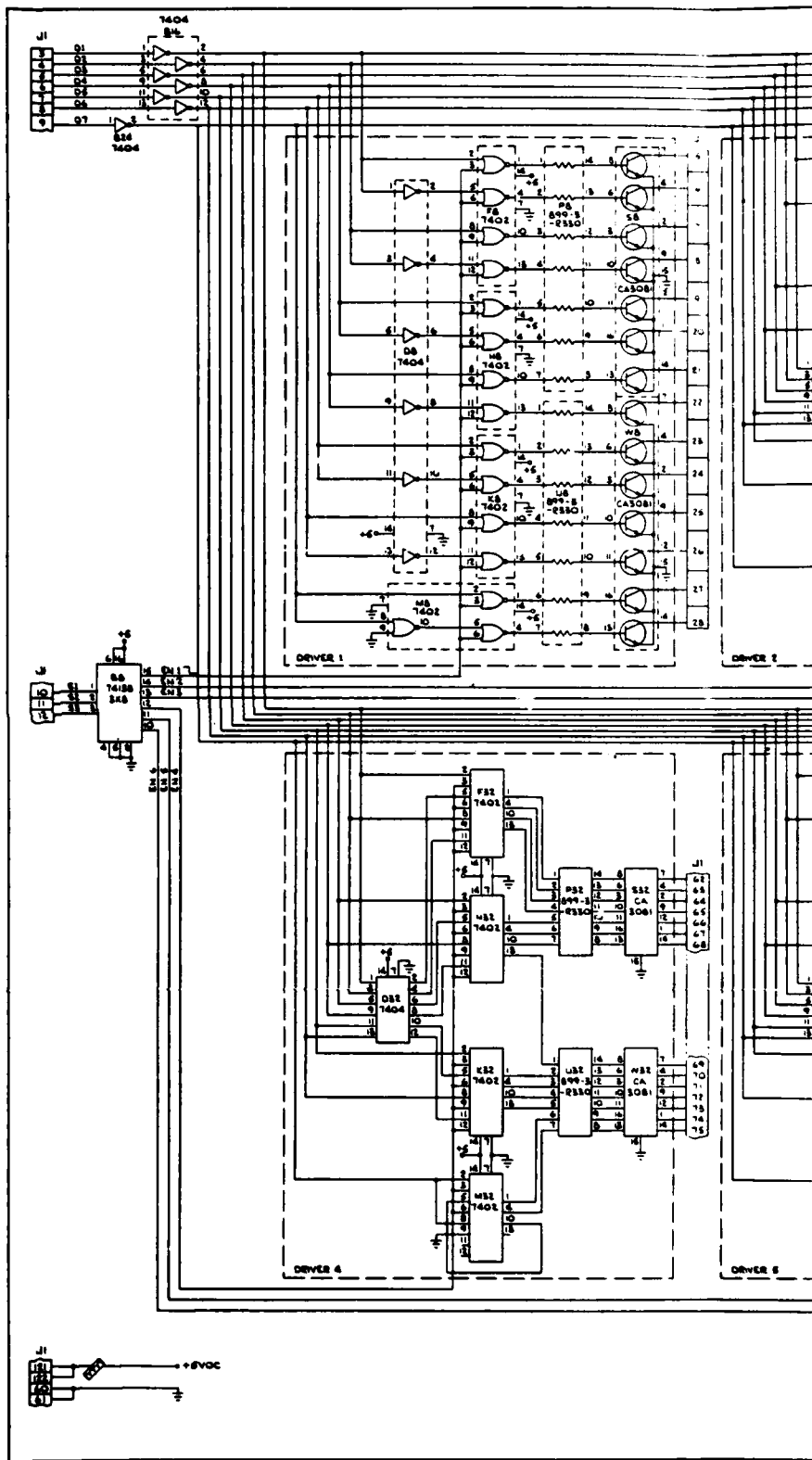
line of B8 (pin 15) will go low to enable driver 1. This enable applied to pins 3 and 6 of F8 combined with the signal from D1 cause the pin 1 output of F8 to go high. This turns on the top transistor in the CA3081 array (S8). The solenoid from the 1 dB attenuator section in RF channel 1 will operate because a ground path has been supplied for the 24 V solenoid coil voltage. The operation of other solenoids controlled by driver 1 or other drivers is identical. A partial schematic of the HP 8495H attenuator is shown in Fig. J-2. The HP 8494H is similar, differing only in value and number of sections.

There is one small address anomaly associated with this card. The addresses for RF channels 1 to 6 are represented by BCD codes 0 to 5, respectively. Codes 6 and above are inactive. Other control cards for other RF channel functions use BCD address codes that match the RF channel number.

On the schematic of this card the chip identification number (i.e., F8 for the 7402 chip) locates pin 1 of that chip on the row-column matrix of pins on the Augat wire-wrap card.

Transient suppression diodes are connected from each solenoid drive transistor's output to both ground and the +24 V solenoid coil voltage supply point. These diodes are mounted on the backplane of the AM/FM/Level-Set card cage and are shown on that schematic (Fig. L-1). The diodes for one solenoid are shown in Fig. J-2.

Figure J-3 is a photograph of this card.



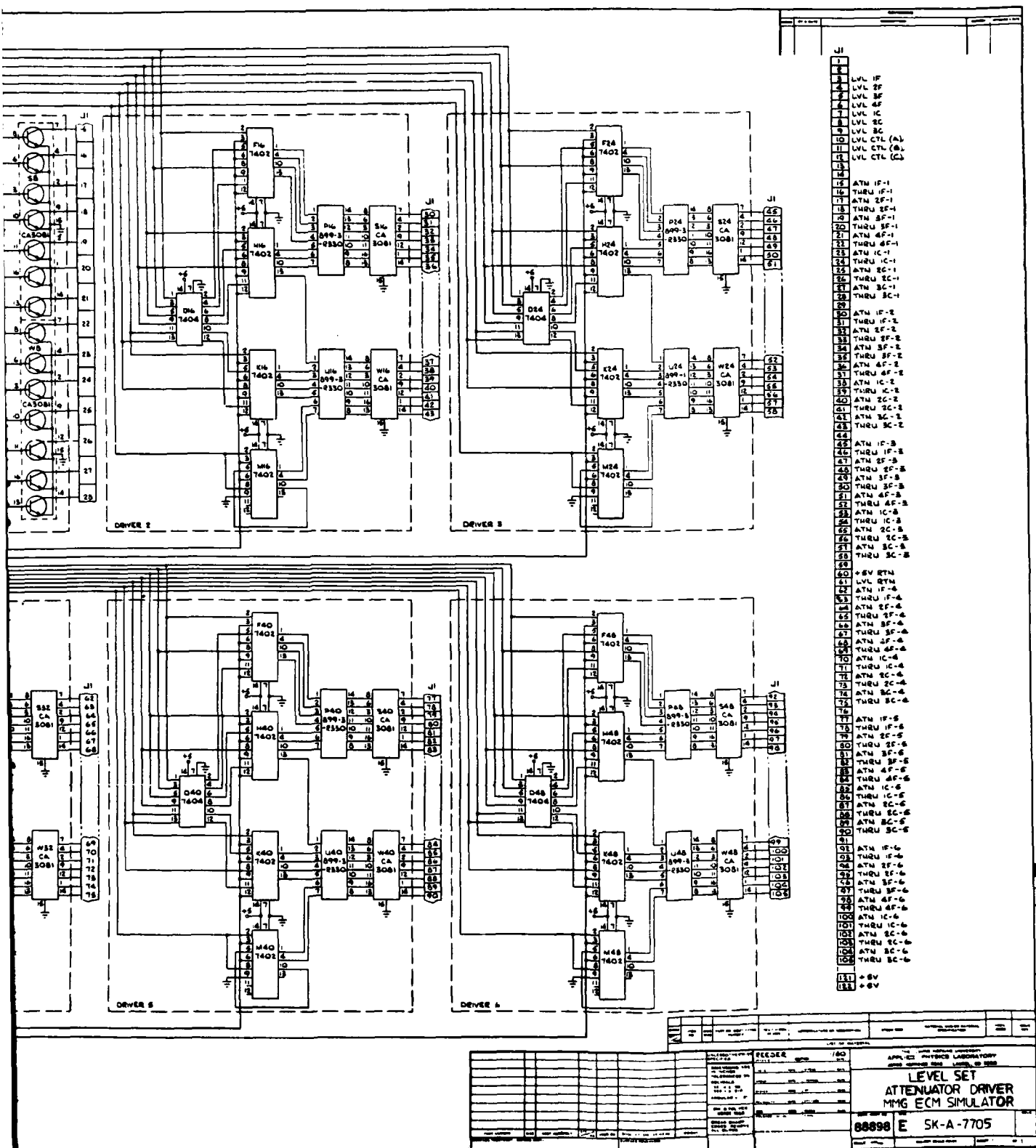


Figure J-1 — Level-set attenuator driver.

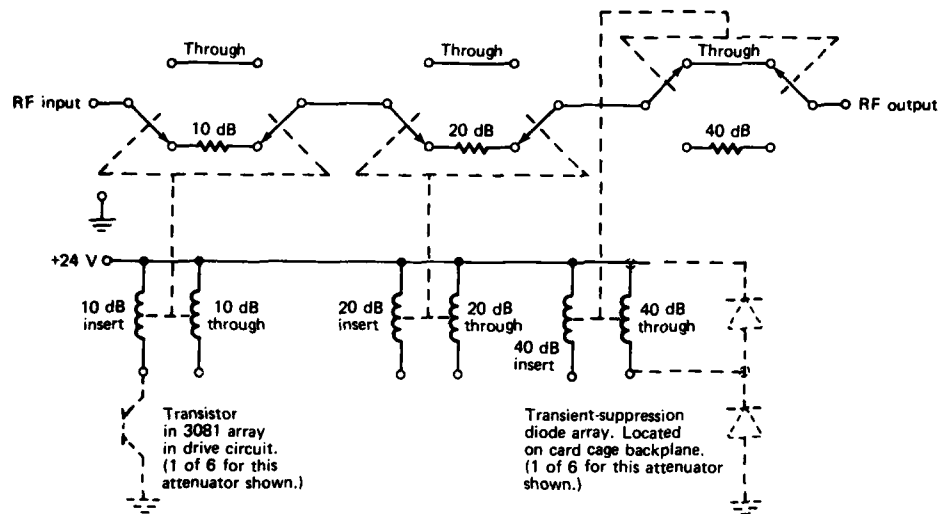


Figure J-2 — Partial schematic of HP 8495H attenuator.

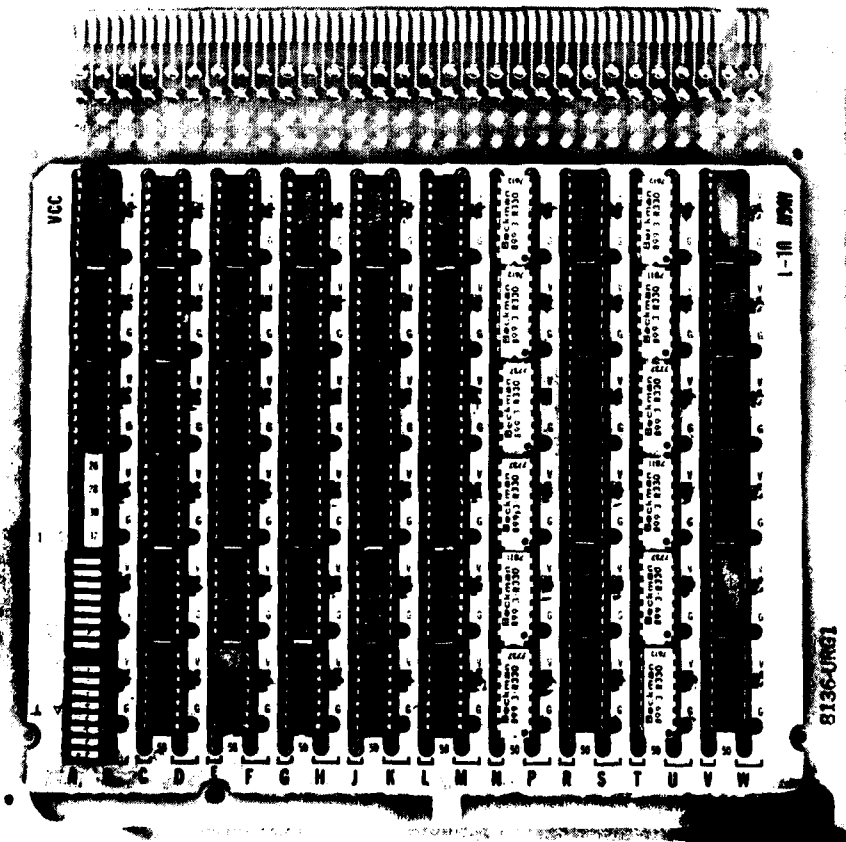


Figure J-3 — Level-set attenuator driver card.

APPENDIX K

COMPONENTS

The MMG Low Frequency ECM Simulator uses several commercial components. These can be divided into two groups. The first group consists of the HP 9825S computer, the HP 6942/6943 multiprogrammer and extender, the Wavetek 175 arbitrary waveform generators, etc. The second group includes RF channel components such as VCO modules, solid state amplifiers, isolators, attenuators, etc.

Most of this second group of components have been discussed in sufficient detail elsewhere in this report and will not be repeated here. Only their relevant specifications are presented in this appendix in tabular form. The VCO modules, however, are discussed, including their specifications and observed characteristics in this application.

HP 9825S Computer

The HP 9825S computer is the primary controller in this system. This is a high-level language desktop computer with a total program memory capacity of 23K bytes (soon to be upgraded to 64K bytes), an integral display, cassette tape drive, and printer. The interface between the HP 9825S and the MMG Low Frequency ECM Simulator system is entirely via the HPIB bus (IEEE-488 standard).

This computer was chosen because it was the most cost-effective model for this application. Several reasons for this section are:

1. The HP 9825S is faster than the HP 9845 or the HP 1000 minicomputers at a cost of one-third or less.
2. The HP 9825S is completely self-contained.
3. The high-level language (HPL), while unique to this machine, is easy to use and contains numerous powerful functions that allow very complex programs to be easily written.
4. The HP 9825S interfaces with other devices via the IEEE-488 standard interface bus, which eliminates the requirement for special interface hardware construction.

Programs for the HP 9825S are loaded via either the keyboard or the cassette tape drive and are executed immediately, since HPL is interpreted. An assortment of programs and general subroutines has been written that allow an operator, after only a min-

imal amount of instruction, to command the ECM simulator to generate the desired simulated jamming spectrum. The software description for the Low Frequency ECM Simulator is described in Volume B of this report.

Multiprogrammer and Extender

The HP 6942 multiprogrammer and HP 6943 multiprogrammer extender are used as a interface between the HP 9825S and the simulator hardware. The HP 6942 and HP 6943 are each capable of holding up to 16 interface cards of several different types. Three card types are used for control and modulation purposes; the digital output card, the digital-to-analog converter card, and the timer/pacer card.

Eleven digital output cards are used to supply control signals to the system. These cards provide a 16 bit latched TTL-level word at their edge connectors. Three digital output cards are used to supply the 8 bit tuning words to the 6 RF channels. Since each RF channel requires a 16 bit control word, six more cards are used to provide the RF channel control words. Two additional cards control the level-set attenuator and the AM and FM modulation switch matrixes.

One timer/pacer card serves as an optional programmable pulse generator to drive the pulse modulator in the RF channels. This card generates a 50% duty cycle square wave having periods ranging from 1 μ s to 18 hours under control of the HP 9825S. At this time, the 6 RF channels share the timer/pacer card with the appropriate channels being connected by the pulse modulation selector card.

Seven digital-to-analog converter cards are used as modulation sources for both FM and AM modulators. One D/A card is shared by up to six RF channels to provide frequency modulation of the VCO's. The remaining six D/A converter cards are used to provide an independent amplitude modulation source for each RF channel. These D/A cards can be controlled by the HP 9825S to generate a range-run-down program.

Arbitrary Waveform Generators

Two Wavetek Model 175 arbitrary waveform generators are used in the system to provide sources of

AM, FM, and pulse modulation. These devices are versatile function generators that can produce sine, square, triangle, and ramp waveforms at rates to 20 kHz. In addition, they can be programmed to produce any arbitrary waveform that can be described in amplitude as a function of time. The maximum bandwidth of the arbitrary waveform is restricted to 2 MHz. All programming and control communication between the HP 9825S and the Wavetek 175 is over the IEEE-488 standard interface bus.

Voltage-Controlled Oscillators

The VCO modules are nonlinearized units manufactured by Texscan Corporation. The type I RF channels use the VTS-25 and the VTS-50 modules, which cover 250 to 500 MHz and 500 to 1000 MHz, respectively. The type II RF channel, which covers 1 to 4 GHz, uses the VTO-100 and VTO-200 oscillators.

Specifications for these modules are listed in Table K-1. These VCO modules were selected because, at the time, they represented the most cost-effective solution to the problem of obtaining octave-band VCOs that could be modulated by wideband signals.

These VCO's have nonlinear tuning curves of frequency as a function of voltage. The nonlinear tuning curves can produce some unusual spectral phenomena that deserve special mention. Although these phenomena are interesting, they are well within the $\pm 10\%$ tuning linearity specified for the VTS-25 and the VTS-50 modules and the 10% tuning linearity specified for the VTO-200. They also only minimally impact the generation of test ECM spectra, since realistic jammers would not usually go to excessive lengths to generate clean RF carrier signals which are then frequently modulated with noise. These phenomena are discussed because they exist in the present system.

Table K-1 - VCO Specifications.

VTS-25		VTO-100	
Frequency range	250 to 500 MHz	Frequency range	1 to 2 GHz
Power output	400 mW into 50 Ω	Power output	50 mW into 50 Ω
Power variation over frequency range	2 dB	Power variation over frequency range	6 dB
Bias	-30 V @ 200 mA (typical)	Bias	-24 V @ 150 mA (typical)
Tuning voltage range	0 to 30 V	Tuning voltage range	-6 to -65 V
Tuning linearity	$\pm 10\%$	Tuning linearity	10%
Modulation video bandwidth	greater than 5 MHz	Modulation video bandwidth	approximately 20 MHz
VTS-50		VTO-200	
Frequency range	500 MHz to 1 GHz	Frequency range	2 to 4 GHz
Power output	400 mW into 50 Ω	Power output	50 mW into 50 Ω
Power variation over frequency range	2 dB	Power variation over frequency range	6 dB (typical)
Bias	-30 V @ 200 mA (typical)	Bias	-24 V @ 150 mA (typical)
Tuning voltage range	0 to 30 V	Tuning voltage range	-12 to -65 V
Tuning linearity	$\pm 10\%$	Tuning linearity	10%
Modulation video bandwidth	greater than 10 MHz	Modulation video bandwidth	>20 MHz
Specifications common to both the VTS-25 and VTS-50 VCO modules		Specifications common to both the VTO-100 and VTO-200 modules	
Signal-to-harmonic ratio	≥ 15 dB	Signal-to-harmonic ratio	15 dB, minimum; 20 dB, typical
Nonharmonic spurious rejection	≥ 50 dB	Nonharmonic spurious rejection	65 dB (typical)
Frequency pulling (1.3:1 VSWR)	$\pm 5\%$	Frequency pulling (1.3:1 VSWR)	$\pm 2\%$ (typical)
Frequency drift	250 ppm/ $^{\circ}$ C	Frequency drift	255 ppm/ $^{\circ}$ C (typical)
Amplitude drift (-30 to +60 $^{\circ}$ C)	1 dB	Amplitude drift (-30 to 60 $^{\circ}$ C)	1 dB (typical)
Frequency pushing (Δf for ΔV bias)	1%/V (typical)	Frequency pushing (Δf for ΔV bias)	1%/V (typical)

The simplest effect is that produced by the S-shaped curve illustrated in Fig. K-1. Using linear scales on the ordinate and abscissa, it is easily seen that the same magnitude of voltage change in the range V_L to V_1 or V_2 to V_H will produce a much smaller change in frequency than the same voltage change in the range V_1 to V_2 . This effect will cause the deviation (and hence the RF spot bandwidth) to change as the DC component of the tuning voltage changes over this range, while the AC modulating voltage superimposed on the DC level remains constant. A 4:1 change in the RF spot bandwidth for a constant modulating voltage amplitude was not unusual.

A second phenomenon is illustrated in Fig. K-2. In this case, the nonlinearity in the curve has become almost a step change in frequency as a function of voltage. The observed frequency step is typically 5 to 10 MHz for a voltage change of 1 mV in VCO's that display this phenomenon. The effect of this phenomenon is to produce a hole in the VCO output spectrum as the tuning voltage is swept in a linear fashion.

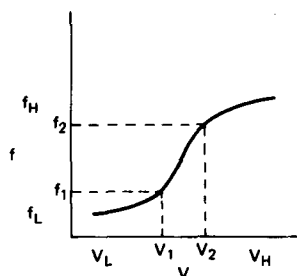


Figure K-1 — Nonlinear f versus V VCO tuning curve.

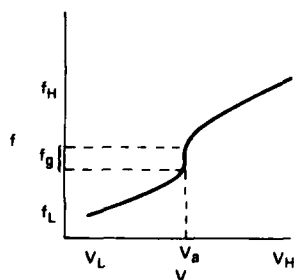


Figure K-2 — Step phenomenon in VCO tuning curve.

For example, the frequency output of the VCO for a tuning voltage of exactly V_a (Fig. K-2) is not well defined. The magnitude of noise on the tuning

voltage exceeds 1 mV, and an attempt to set exactly V_a as a tuning voltage will result in a situation where the VCO output frequency rapidly switches from the upper to the lower limits of the range F_R . In effect, the VCO is being modulated by a square wave. The spectrum generated in this case may "fill in" the discontinuity with a noise-like spot during the time the tuning voltage is nearly equal to V_a .

This "fill in" effect will reduce or eliminate the discontinuity in the VCO RF output spectrum when a wideband noise-like spot is requested. However, this same effect will cause a broadband spot to be generated during a slow sweep of a narrowband RF spot.

Another phenomenon of interest observed combines the step phenomenon with a hysteresis effect (Fig. K-3). In this case, the VCO output frequency increases as the tuning voltage increases until V_a is reached; at that point a step change in frequency occurs. Further increases in the tuning voltage produce smooth increases in frequency. If the tuning voltage is reversed the VCO output frequency will smoothly decrease until V_b is reached, at which time the frequency will decrease in a step fashion. Further decreases in the tuning voltage will cause smooth decreases in frequency.

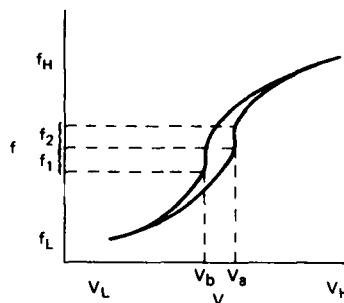


Figure K-3 — Step phenomenon with hysteresis in VCO tuning curve.

These step changes in frequency are on the order of 5 to 10 MHz and, for those modules that display this phenomenon (usually the 250 to 500 MHz units), the steps do not coincide in frequency. This means that although the frequency exhibits steps or gaps for linear voltage sweeps in both the increasing and decreasing directions, when these sweeps occur one after the other the discontinuities in one frequency sweep direction are filled in by the opposite polarity sweep, resulting in full frequency coverage. An operator will usually notice this effect only when a narrow noiselike spot (or CW line) is slowly swept up

and down in frequency over a range that includes the steps.

The nonlinearity in the tuning curve as displayed in Fig. K-1 is included in the calibration program. This allows the operator to request a desired noise spot bandwidth at any center frequency in the VCO range. The HP 9825S will compute the proper noise and fill attenuation levels to generate a spot whose bandwidth is as close as possible to the desired bandwidth. For the prewritten programs this operation is transparent to the operator. The effects of the steps in Figs. K-2 and K-3 are not corrected in software.

Tables K-2 through K-8 list the important specifications of the component modules used in the MMG Low Frequency ECM Simulator.

Table K-2 – Pulse Modulator Specifications.

Alpha Industries MT3586A

Use: pulse modulation

Nonreflective SPDT PIN diode switch

Frequency range	0.5 to 4 GHz
Insertion loss	≤ 1.6 dB
VSWR ratio	$\leq 1.5:1$
Isolation	> 65 dB
Time rise (10 to 90% RF), maximum	125 ns, typical; 500 ns,
Time fall (90 to 10% RF), maximum	550 ns, typical; 1000 ns,
Time on (50% TTL to 90% RF)	155 ns (typical)
Time off (50% TTL to 10% RF)	700 ns (typical)
Integral TTL driver	
logic 1	J1 \rightarrow J3
logic 0	J1 \rightarrow J2

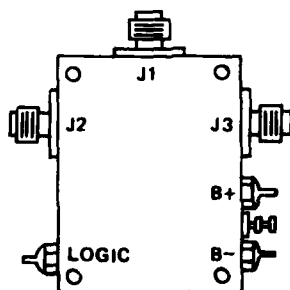


Table K-3 – Amplitude Modulator Specifications.

Linear analog PIN diode absorptive attenuators

Use: linear amplitude modulation

Anaren 60464 and 60466, voltage-controlled models.

60464	
Frequency range	0.5 to 1 GHz
Attenuation range	55 dB (minimum)
Attenuation flatness	± 2 dB
Insertion loss	1.5 dB (maximum)
VSWR	1.5:1 (maximum)
Attenuation drive voltage	0 to +10 V

60466	
Frequency range	2 to 4 GHz
Attenuation range	55 dB (minimum)
Attenuation flatness	± 2 dB
Insertion loss	2 dB (maximum)
VSWR	1.6:1 (maximum)
Attenuation drive voltage	0 to ± 10 V

Linearizer Anaren 300010

Use: Used with Anaren 60464 and 60466 PIN diode attenuators to produce a linear attenuation versus voltage curve.

These units are factory aligned with an attenuator to give a linear attenuation curve with a slope of 5.5 dB/V ± 1 dB.

Table K-4 – Biphase Modulator Specifications.

Use: biphase modulation

Type I RF channel

Watkins-Johnson M1J double-balanced mixer

LO, RF ports frequency range	300 to 2000 MHz
IF port frequency range	DC to 1 GHz
L-R isolation	40 dB (minimum)
Conversion loss	7 dB (maximum)
Drive level (IF port)	+4 dBm minimum +13 dBm maximum

Type II RF channel

Summit 1307 double-balanced mixer

LO, RF port frequency range	1 to 4.2 GHz
IF port frequency range	DC to 1 GHz
L-R isolation	1 to 3 GHz, 35 dB; 3 to 4.2 GHz, 25 dB
Conversion loss	1 to 1.5 GHz, 8 dB; 1.5 to 4.2 GHz, 7 dB
Drive level (IF port)	+7 dBm, nominal; +10 dBm, maximum

Table K-5 — RF Amplifier Specifications.

Use: RF Output Amplifier

Type I RF channel

Avantek UTC 12-104

Frequency range	10 to 1000 MHz
Gain	26 dB
Noise figure	≤4.5 dB
Power output @ 1 dB compression	+20 dBm
Gain flatness	±1.5 dB
IM intercept point	+33 dBm
VSWR (50 Ω) in and out	2:1
Power	+15 V @ 180 mA (typical)

Type II RF channel

Watkins-Johnson 6614501

Frequency range	1 to 4 GHz
Gain	≥18 dB
Noise figure	≤6 dB
Power output @ 1 dB compression	+23 dBm
Gain flatness	±1 dB
IM intercept point	+32 dBm
VSWR (50 Ω) in and out	2:1
Power	+15 V @ 220 mA

Table K-7 — RF Sampler Specifications.

Use: Provide front panel RF sample

Omni spectra 203836-10,

50 Ω bilateral resistive sampler

Frequency range	1 to 12.4 GHz
Coupling	20 dB
Coupling variation	±1.5 dB
Main line VSWR	1.5:1
Insertion loss	1 dB (maximum)

Table K-6 — Coaxial Step Attenuator Specifications.

Use: Level-set Attenuators

Hewlett-Packard 8494H coaxial step attenuator

Attenuation range	0 to 11 dB in 1 dB steps	
Frequency range	DC to 18 GHz	
VSWR (DC to 8 GHz)	1.5:1	
Insertion loss	0.6 dB + 0.9 (f _{GHz}) dB	
Attenuation accuracy	Attenuation	Accuracy
(DC to 12.4 GHz)	1 to 2 dB	± 0.4 dB
	3 to 4 dB	± 0.4 dB
	5 to 6 dB	± 0.5 dB
	7 to 10 dB	± 0.6 dB
	11 dB	± 0.7 dB

Solenoid characteristics

Voltage	20 to 30 V
Switching speed	20 ms (maximum)
Power	2.7 W
Attenuator power rating	1 W (average)

Hewlett Packard 8495H coaxial step attenuator

Specifications same as 8494H (above) except

Attenuation range	0 to 70 dB in 10 dB steps
VSWR (DC to 8 GHz)	1.35:1
Insertion loss	0.4 dB + 0.07 (f _{GHz}) dB
Attenuation accuracy	greater of 3% or ±1.7 dB of setting

Table K-8 — Noise Module Specifications.

Use: Gaussian Noise Source

Micronetics 1000MSD-2L

Frequency range	10 Hz to 10 MHz
Output	1000 mV into 50 Ω
Power supply	+15 V
Spectral flatness within band	2.5 dB
Roll-off outside band	approximately 6 dB/octave
Peak/RMS ratio	5:1

APPENDIX L

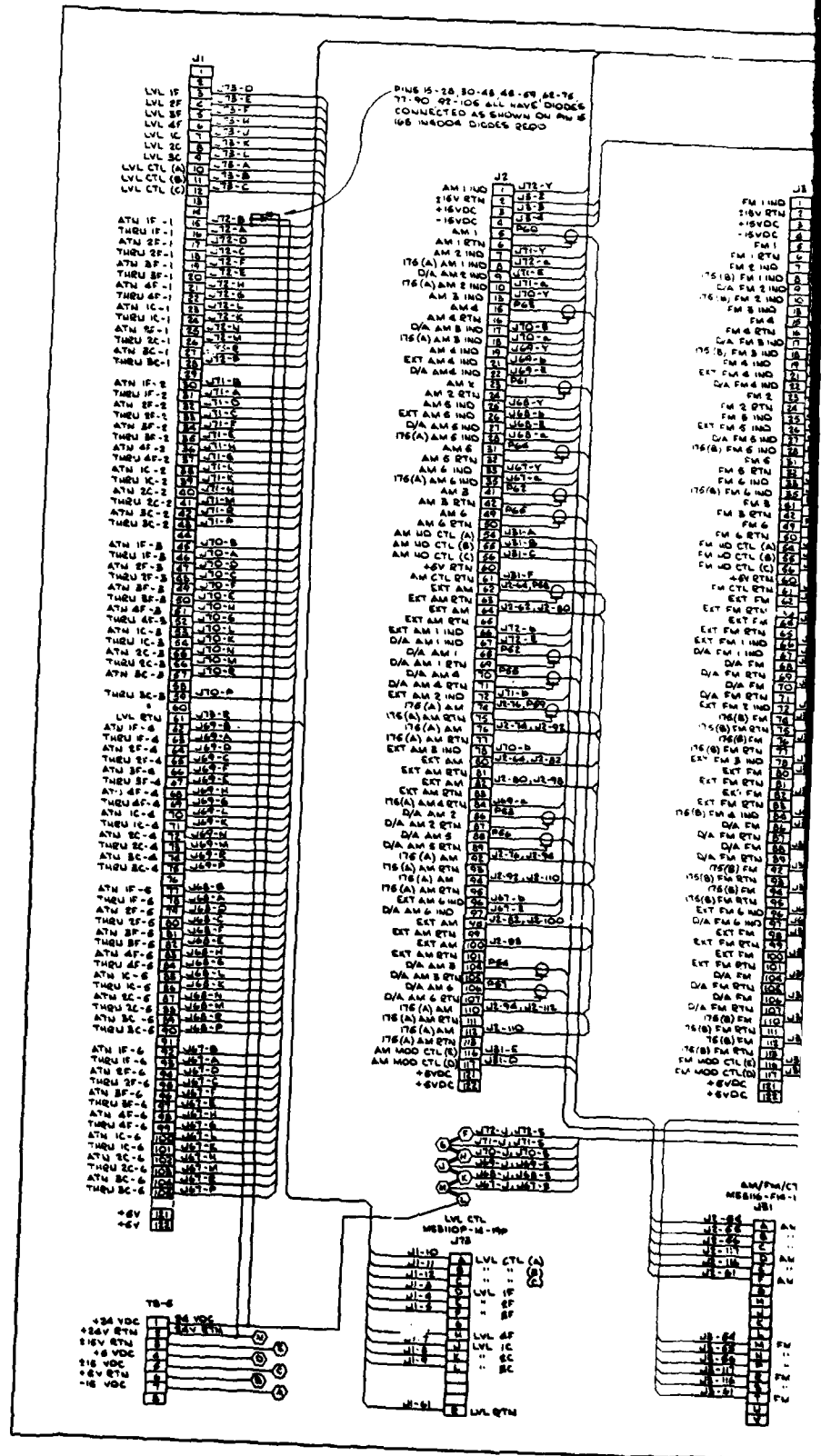
THE AM/FM LEVEL-SET CARD CAGE (AUGAT CARD CAGE)

Figure L-1 shows the wiring diagram of the AM/FM Level-Set Card Cage (Augat card cage). This chassis holds the AM modulation switch matrix card, the FM modulation switch matrix card, and the level-set driver card. The chassis also holds a +5 V power supply for the TTL logic on these cards, a ± 15 V power supply for the analog buffers on these cards and, a +24 V power supply for the HP 8494H and HP 8495H level-set attenuators in the RF channels.

The chassis is mounted on slide-out rails in the rear of the MMG Low Frequency ECM Simulator rack. Figures L-2 through L-5 are photographs of the chassis.

Mounted above the Augat card cage in the rear of the equipment rack is a patch panel that provides ready access to the two Wavetek output ports. Figure L-6 is a photograph of this panel.

The SMA connectors are all simple bulkhead connectors with the exception of the AM Pulse outputs. These six output connectors are connected in parallel across the Pulse In connector. Signals from the pulse outputs are routed to the appropriate RF channels from these connectors.





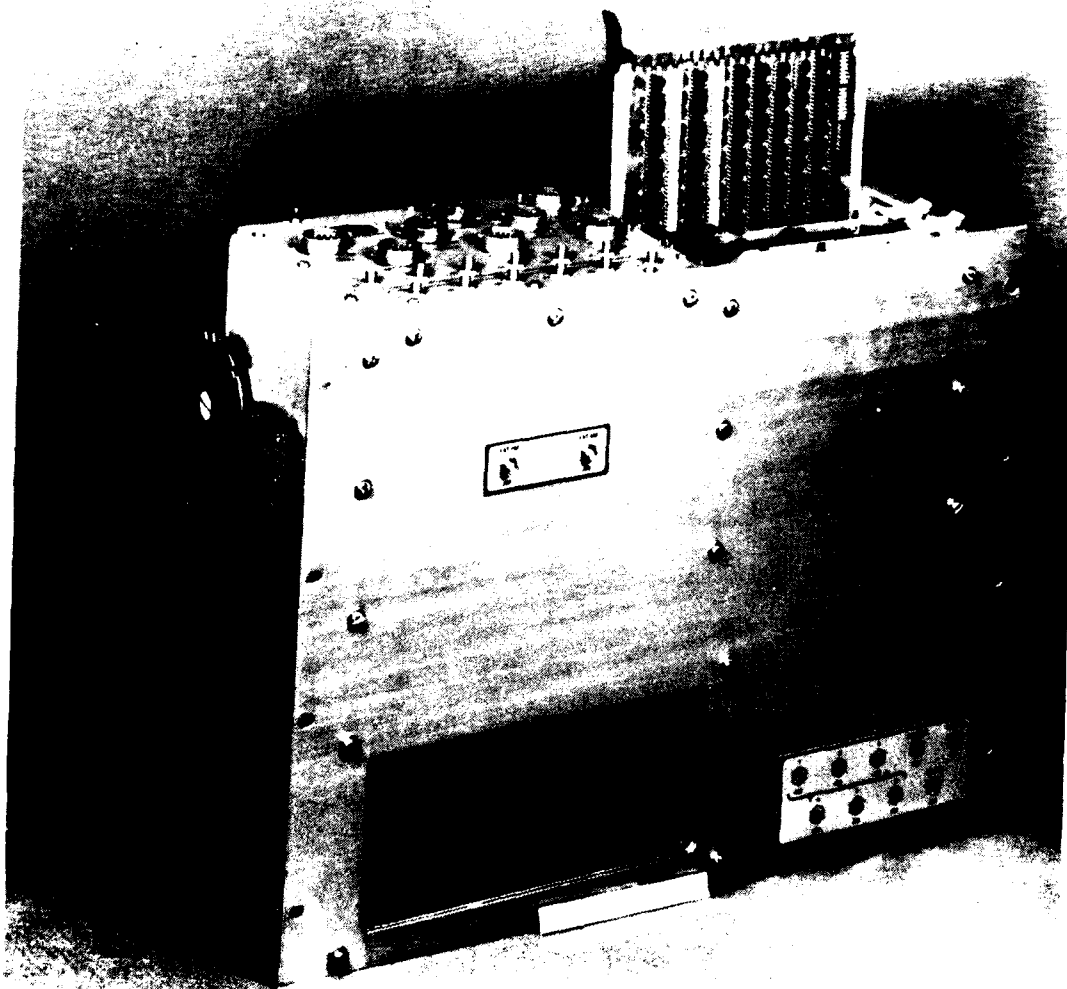


Figure L-2 — AM/FM level-set card cage chassis, front view.

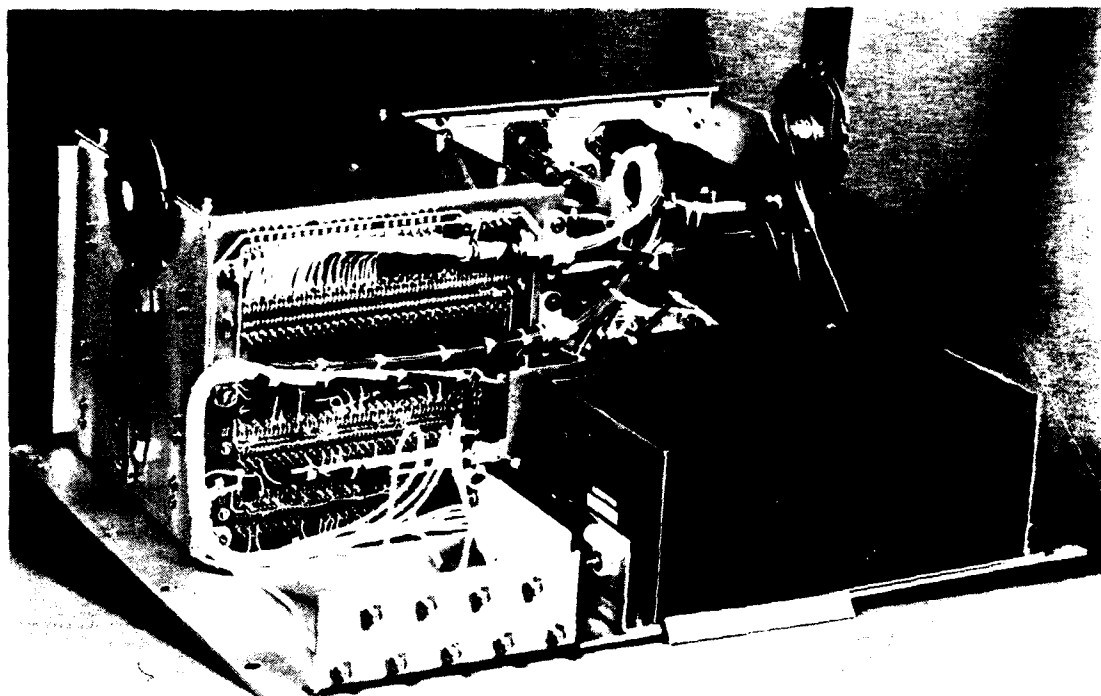


Figure L-3 — AM/FM level-set card cage, left rear view.

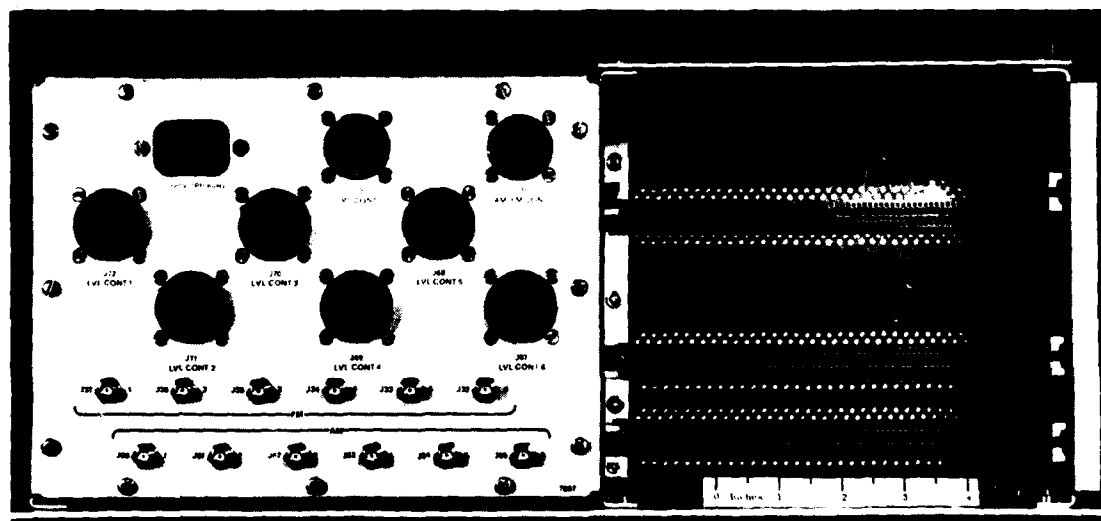


Figure L-4 — AM/FM level-set card cage, top view.

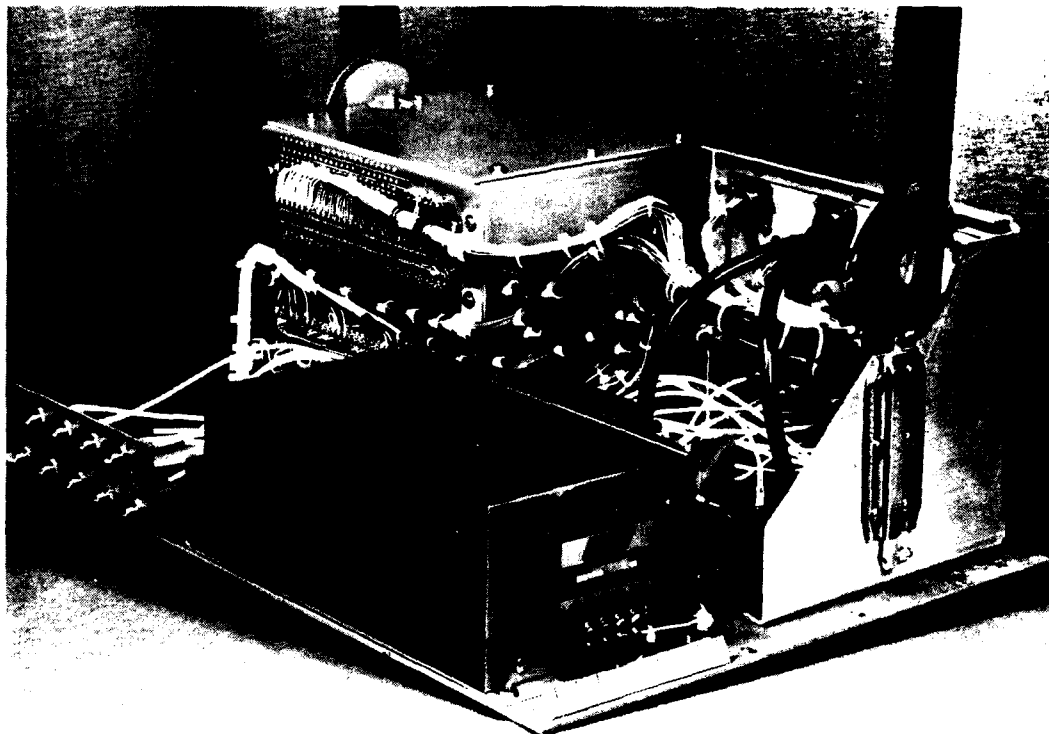


Figure L-5 — AM/FM level-set card cage, right rear view.

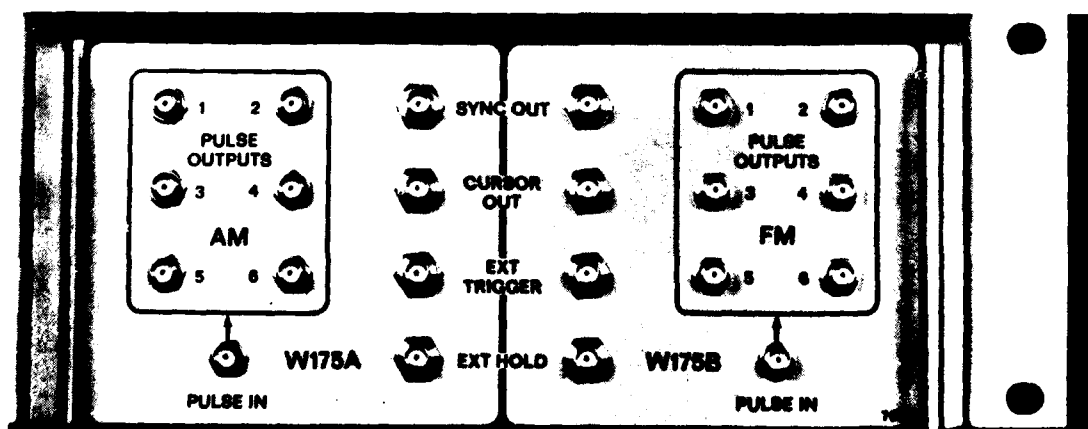


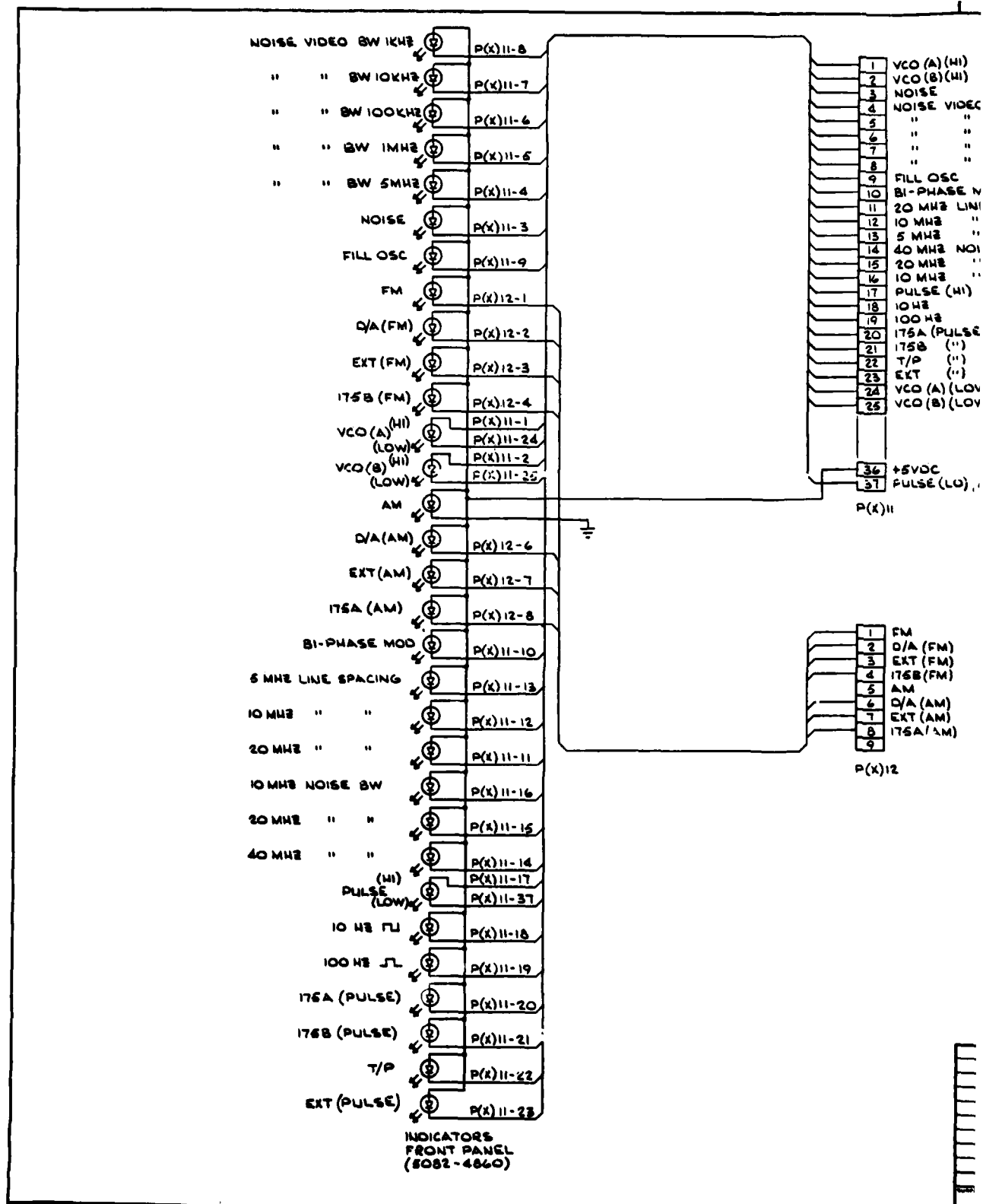
Figure L-6 — Patch panel.

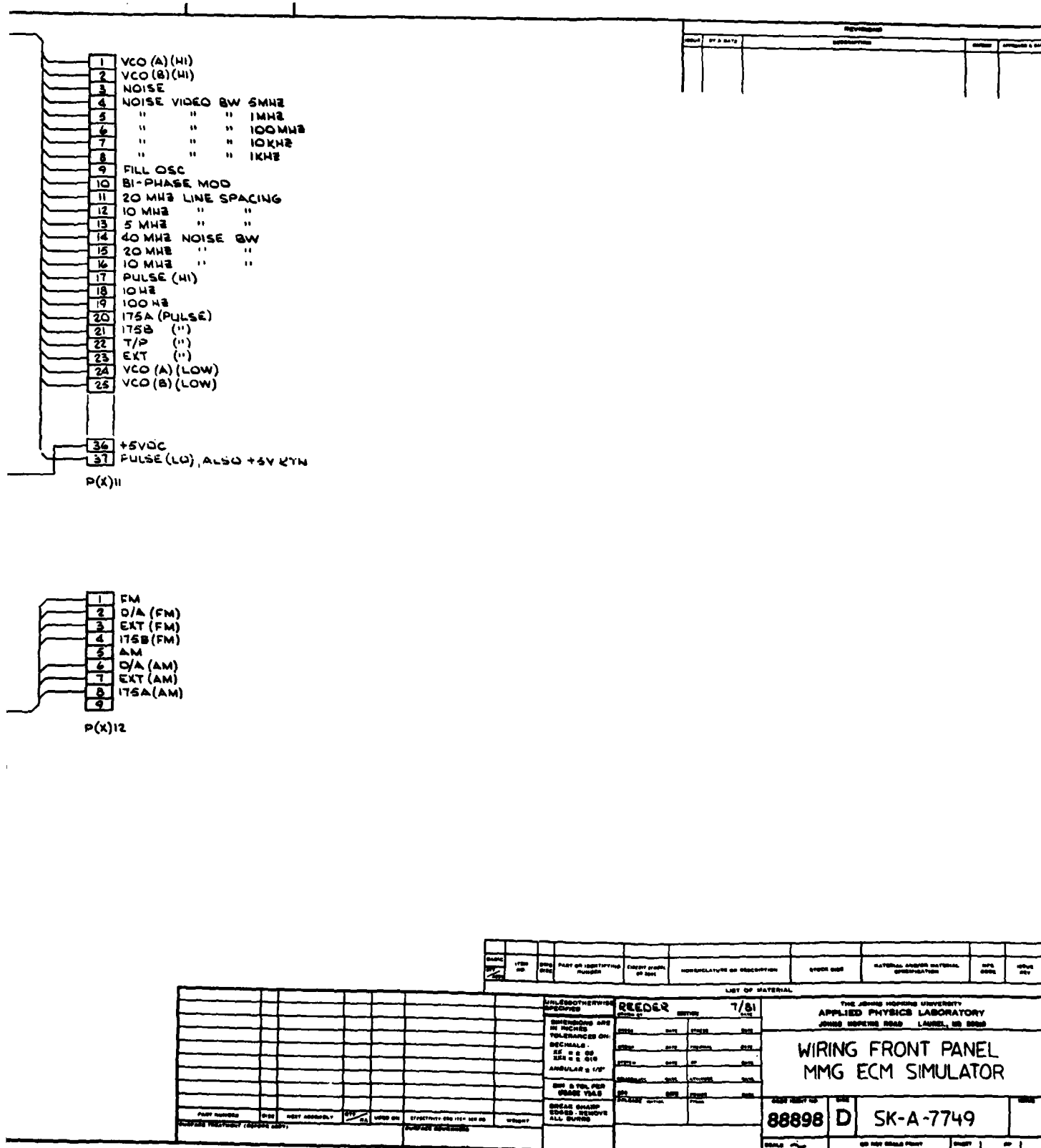
APPENDIX M

FRONT PANEL

The front panel of each RF channel in the MMG Low Frequency ECM Simulator has a block diagram etched on its face. Light-emitting diodes in each block indicate to an operator which blocks are active and, where applicable, the mode of the active block.

Figure M-1 is the schematic of the front panel.



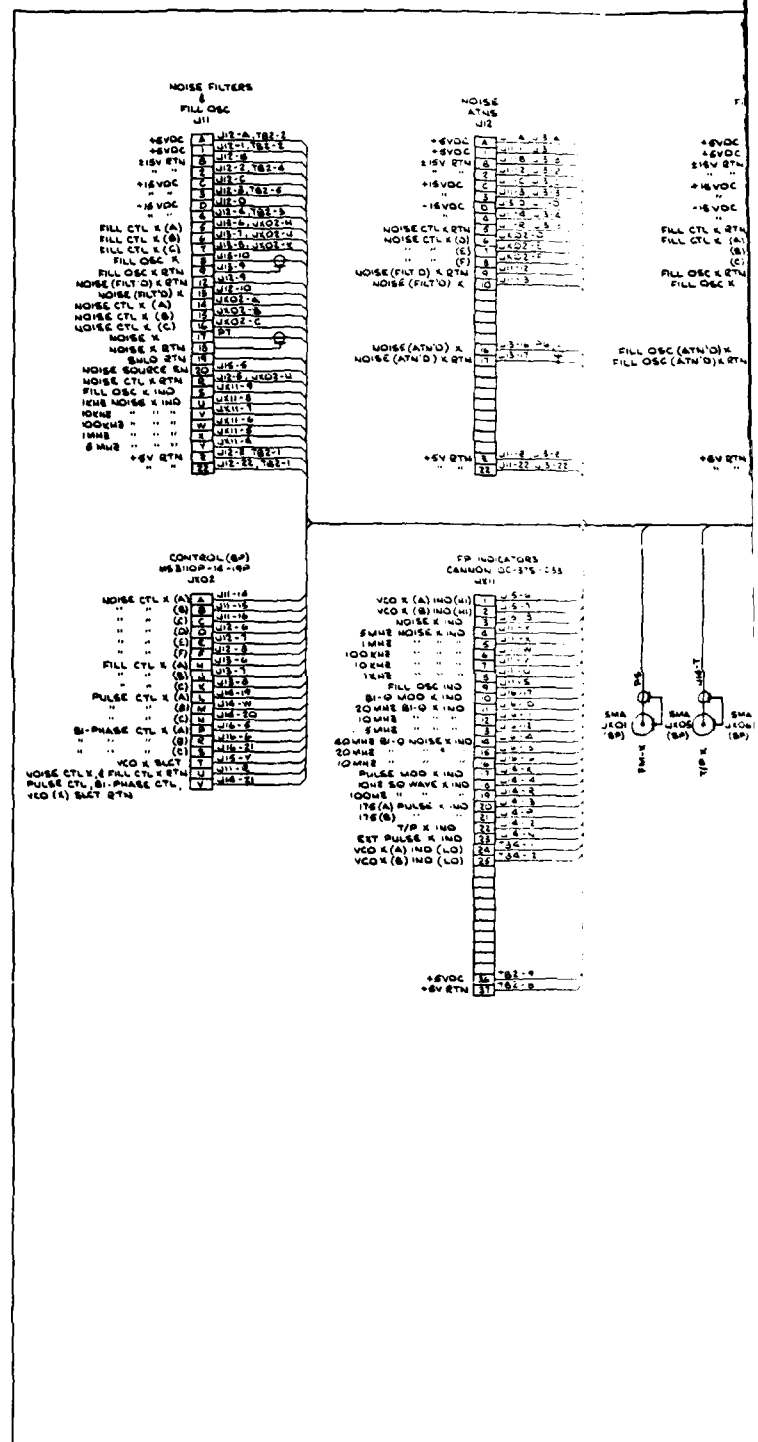


APPENDIX N

RF CHANNEL CARD CAGE WIRING DIAGRAM

The wiring diagram for the wire wrap card cage in each RF channel is shown in Fig. N-1. The wiring is identical for the type I and type II RF Channels.

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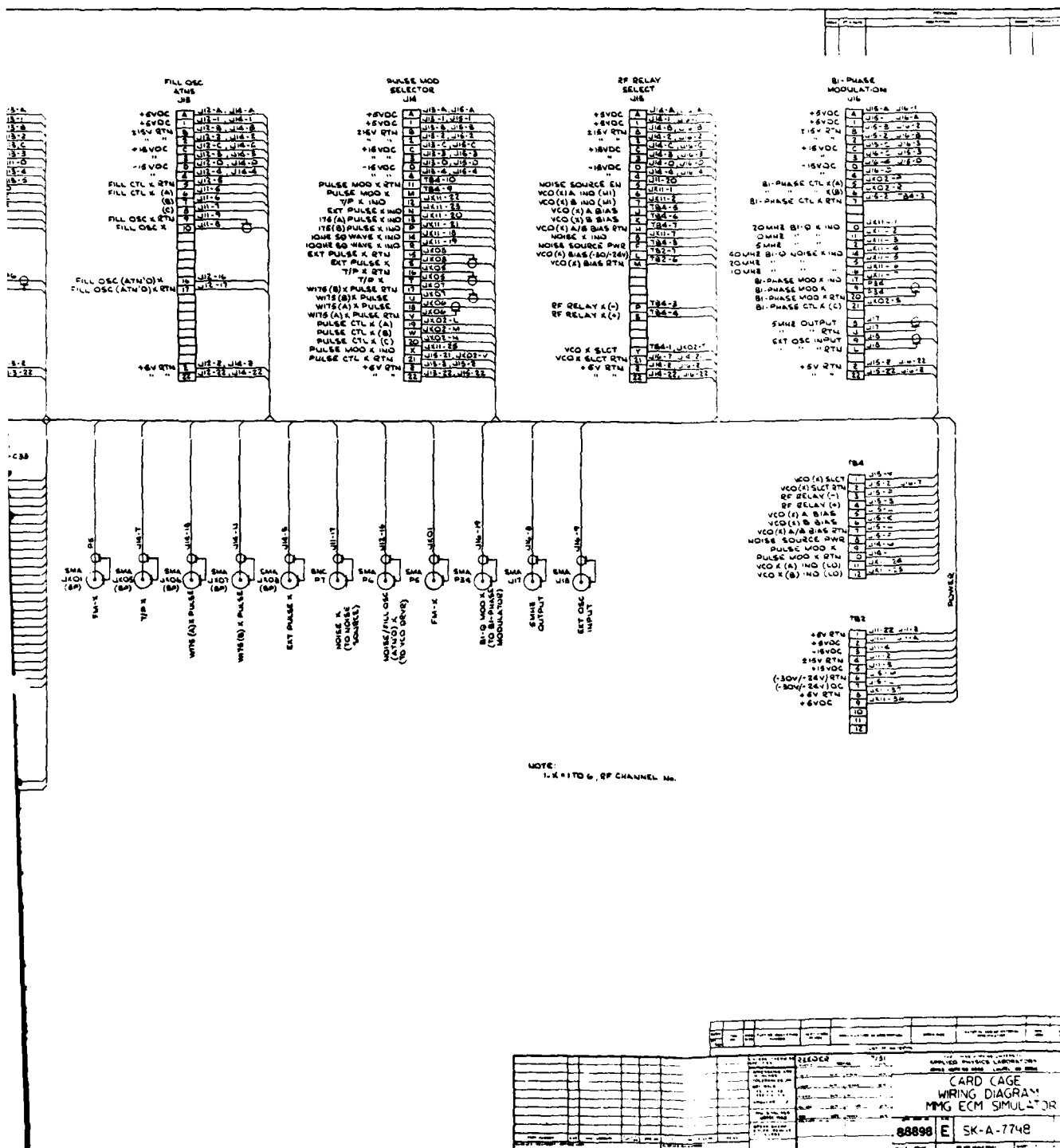


Figure N-1 — Card cage wiring diagram.

APPENDIX O

POWER SUPPLY ASSEMBLY SCHEMATICS

The schematics of the Type I and Type II power supply assemblies are shown in Figs. O-1 and O-2, respectively.

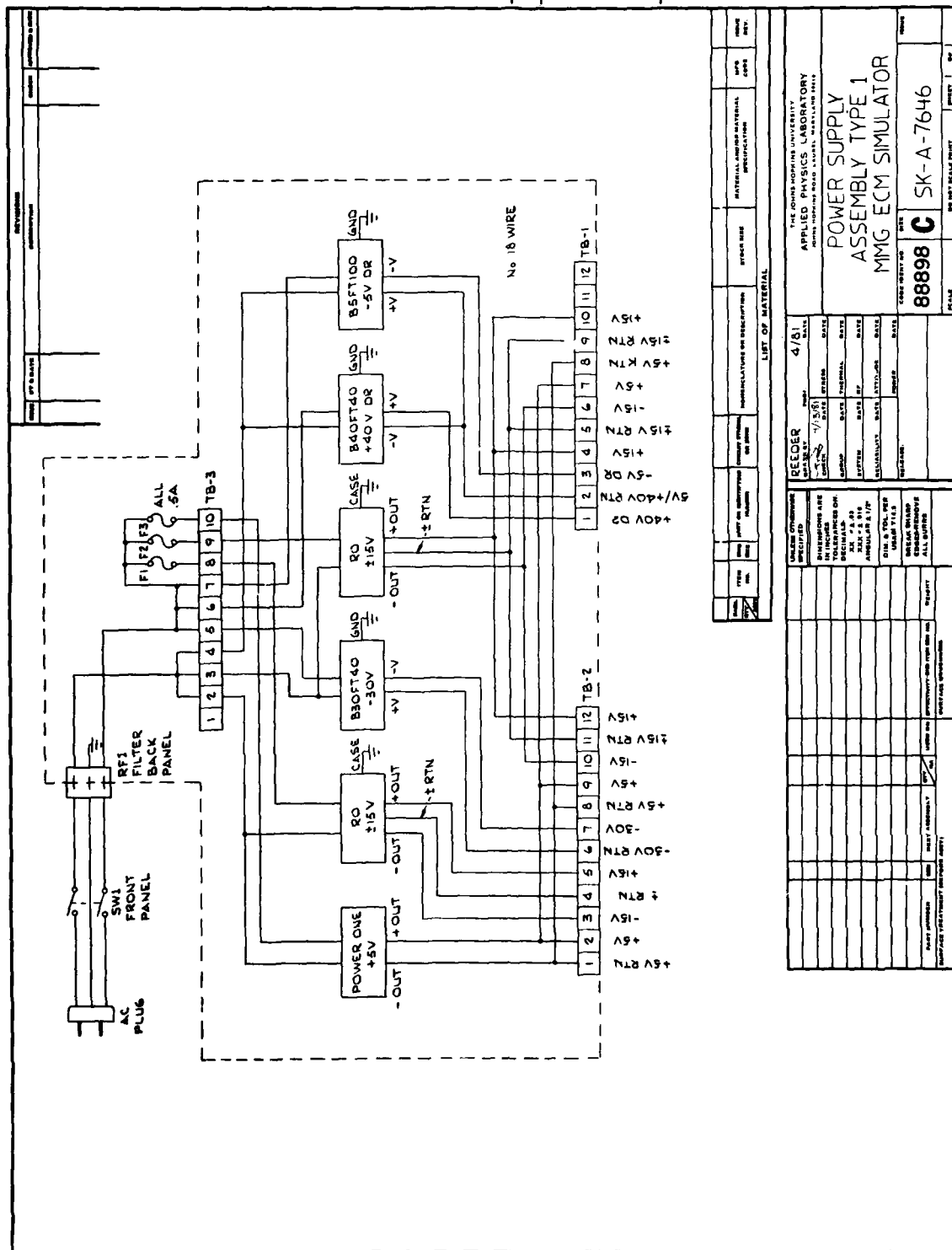


Figure U-1 — Power supply assembly, type I.

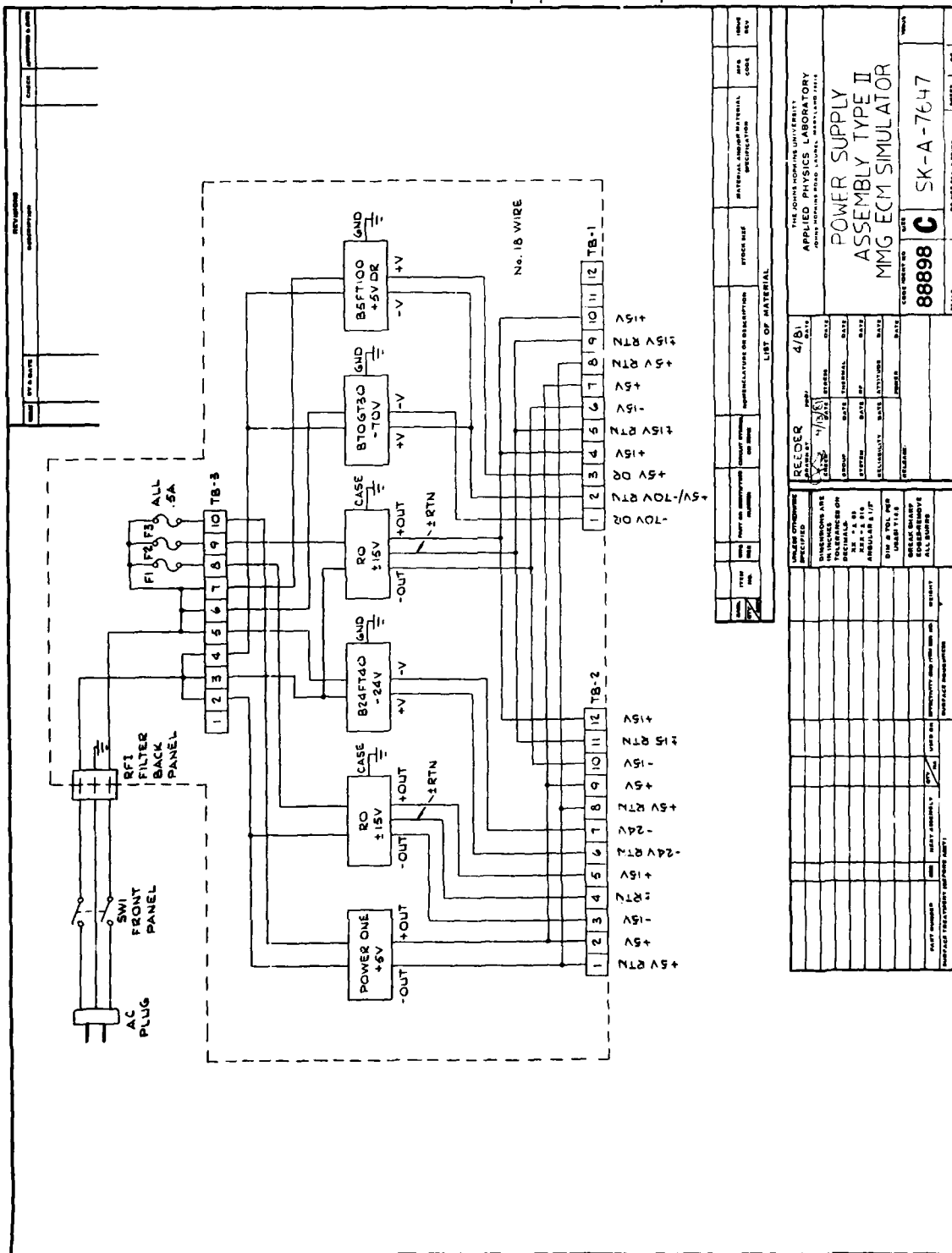


Figure 0-2 — Power supply assembly, type II.

AD-A122 841

MULTIMODE GUIDANCE PROJECT LOW FREQUENCY SCM SIMULATOR:

2/2

HARDWARE DESCRIPTION(U) JOHNS HOPKINS UNIV LAUREL MD

APPLIED PHYSICS LAB M N KAYE OCT 82 JMJ/APL/76-1338A

UNCLASSIFIED

NO0024-83-C-8301

7/8 9/2

NL

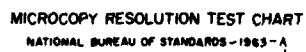
END

DATE

FILMED

2 83

DT

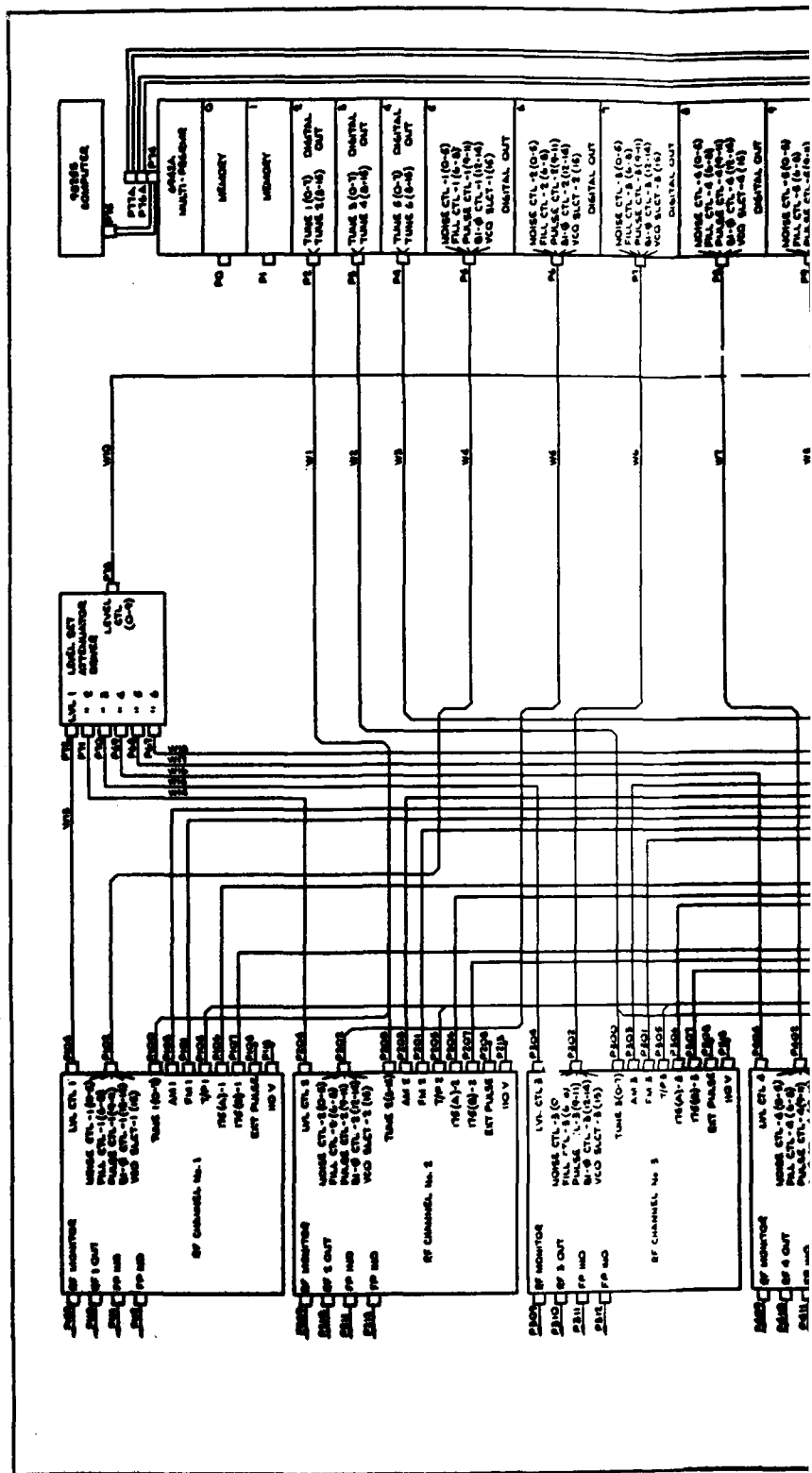


MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

APPENDIX P

INTER-RACK CABLING

The cabling between assemblies is shown in Fig. P-1. The individual cable assemblies (numbers W-1 through W-26) are shown in Figs. P-2 through P-20.





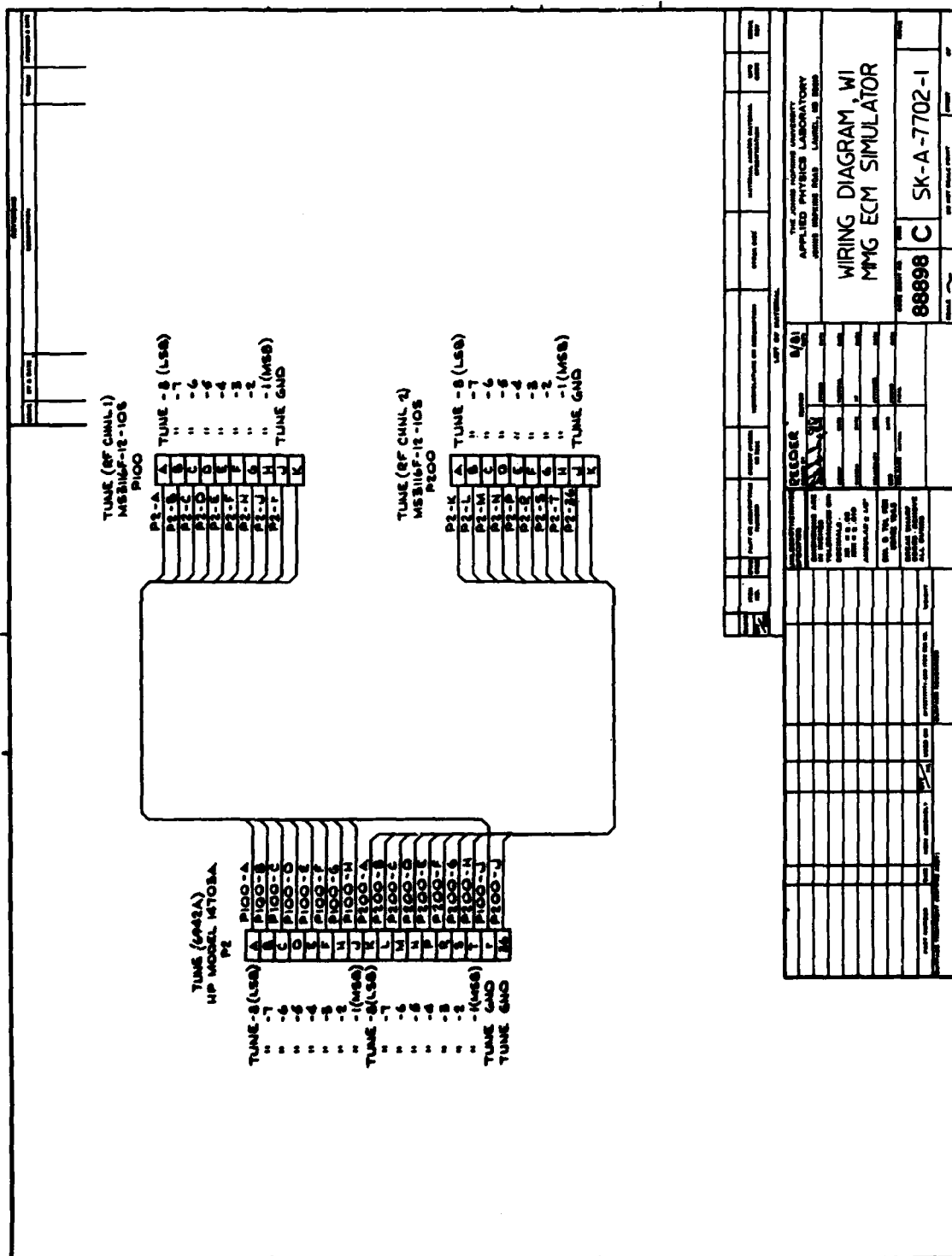


Figure P-2 — Wiring diagram, W-1.

102

TUNE -8 (LSB)	A	P500-A
" -7	B	P500-B
" -6	C	P500-C
" -5	D	P500-D
" -4	E	P500-E
" -3	F	P500-F
" -2	H	P500-G
" -1 (MSB)	J	P500-H
TUNE -8 (LSB)	K	P600-A
" -7	L	P600-B
" -6	M	P600-C
" -5	N	P600-D
" -4	P	P600-E
" -3	R	P600-F
" -2	S	P600-G
" -1 (MSB)	T	P600-H
TUNE GND	Y	P500-J
TUNE GND	36	P600-J

[illegible]

PART NUMBER SIZE NEXT ASSEMBLY QTY UNIT PRICE

SURFACE TREATMENT (BEFORE ASSY)

CONTROL (6942A)
HP MODEL 14703A
P6

NOISE CTL	(A)	A	P202-A
" "	(B)	B	P202-B
" "	(C)	C	P202-C
" "	(D)	D	P202-D
" "	(E)	E	P202-E
" "	(F)	F	P202-F
FILL CTL	(A)	H	P202-H
" "	(B)	J	P202-J
" "	(C)	K	P202-K
PULSE CTL	(A)	L	P202-L
" "	(B)	M	P202-M
" "	(C)	N	P202-N
BI-PHASE CTL	(A)	P	P202-P
" "	(B)	R	P202-R
" "	(C)	S	P202-S
VCO (2) SLCT		T	P202-T
NOISE/FILL CTL RTN		U	P202-U
PULSE, BI-PHASE, VCO SLCT RTN		V	P202-V
		36	

PART NUMBER	QTY	REVT ASSY.	QTY	USED
SURFACE TREATMENT (BORNE COAT)				

6942A)
14703A

CONTROL (RF CHNL 2)
MS3116F-14-195
P202

P202-A
P202-B
P202-C
P202-D
P202-E
P202-F
P202-H
P202-J
P202-K
P202-L
P202-M
P202-N
P202-P
P202-R
P202-S
P202-T
P202-U
P202-V

P6-A	A	NOISE CTL (A)
P6-B	B	" " (B)
P6-C	C	" " (C)
P6-D	D	" " (D)
P6-E	E	" " (E)
P6-F	F	" " (F)
P6-H	H	FILL CTL (A)
P6-J	J	" " (B)
P6-K	K	" " (C)
P6-L	L	PULSE CTL (A)
P6-M	M	" " (B)
P6-N	N	" " (C)
P6-P	P	BI-PHASE CTL (A)
P6-R	R	" " (B)
P6-S	S	" " (C)
P6-T	T	VCO (2) SLCT
P6-U	U	NOISE/FILL CTL RTN
P6-V	V	PULSE, BI-PHASE, VCO SLCT RTN
P6-G	G	

BASIC CITY	ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	CIRCUIT SYMBOL OR CODE	NOMENCLATURE OR DESCRIPTION	STOCK SIZE	MATERIAL AND/OR MATERIAL SPECIFICATION	QTY CODE	ISSUE REV
LIST OF MATERIAL									
UNLESS OTHERWISE SPECIFIED			REORDER		8/81		THE JOHNS HOPKINS UNIVERSITY APPLIED PHYSICS LABORATORY JOHNS HOPKINS ROAD LAUREL, MD 20680		
DIMENSIONS ARE IN INCHES			SECTION		DATE		WIRING DIAGRAM, W5 MMG ECM SIMULATOR		
TOLERANCES ON:			GROUP		DATE				
DECIMALS			SUBMIT		DATE				
XX = ± .05			RELIABILITY		DATE				
ANGULAR ± 1/2°			DATE		ATTITUDE		DATE		
DRL & TOL PER USASI Y14.5			DATE		FOCUS		DATE		
BREAK SHARP EDGES - REMOVE ALL BURRS			RELEASE: INITIAL		FINAL		DATE		
NEXT ASSEMBLY			DATE		DATE		DATE		
EFFECTIVITY: SEE ITEM NO. 10			WEIGHT		CODE IDENT. NO.		SIZE		ISSUE
SURFACE FINISHES					88898 C		SK-A-7702-5		
					SCALE		DO NOT SCALE PRINT		DATE

Figure P-6 — Wiring diagram, W-5.

[illegible]

REVISIONS				
ISSUE	BY & DATE	DESCRIPTION	CHECK	APPROVED & DATE

6942A)
L 14703A

CONTROL (RF CHNL 3)
MS3116F-14-195
P302

P302-A
P302-B
P302-C
P302-D
P302-E
P302-F
P302-H
P302-J
P302-K
P302-L
P302-M
P302-N
P302-P
P302-R
P302-S
P302-T
P302-U
P302-V

P7-A	A
P7-B	B
P7-C	C
P7-D	D
P7-E	E
P7-F	F
P7-H	H
P7-J	J
P7-K	K
P7-L	L
P7-M	M
P7-N	N
P7-P	P
P7-R	R
P7-S	S
P7-T	T
P7-U	U
P7-V	V
P7-G	G

NOISE CTL (A)
" " (B)
" " (C)
" " (D)
" " (E)
" " (F)
FILL CTL (A)
" " (B)
" " (C)
PULSE CTL (A)
" " (B)
" " (C)
BI-PHASE CTL (A)
" " (B)
" " (C)
VCO (3) SLCT
NOISE/FILL CTL RTN
PULSE, BI-PHASE, VCO SLCT RTN

DRAWN BY	ITEM NO.	QTY	PART OR IDENTIFYING NUMBER	CHECK STOCK ON HAND	NOMENCLATURE OR DESCRIPTION	STOCK SIZE	MATERIAL AND/OR MATERIAL SPECIFICATION	QTY CODE	ISSUE REV
LIST OF MATERIAL									
UNLESS OTHERWISE SPECIFIED					REEDER 8/81 THE JOHNS HOPKINS UNIVERSITY APPLIED PHYSICS LABORATORY JOHNS HOPKINS ROAD LAUREL, MD 20080				
DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS: XX = ± .03 XXX = ± .010 ANGULAR ± 1/8° SURF. & TOL PER USAS 13AS BREAK SHARP EDGES - REMOVE ALL BURRS					WIRING DIAGRAM, W6 MMG ECM SIMULATOR				
FIRST APPROVAL BY: <input type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/> USED ON: <input type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/> SPECIFYING AND PER DRG NO. <input type="checkbox"/> SURFACE REQUIREMENTS					CODE IDENT NO: 88898 SIZE: C ISSUE: SK-A-7702-6 SCALE: <input checked="" type="checkbox"/> DO NOT SCALE PRINT: <input type="checkbox"/> SHEET: <input type="checkbox"/> OF: <input type="checkbox"/>				

Figure P-7 — Wiring diagram, W-8.

2

CONTROL (6942A)
HP MODEL 14703A
P8

NOISE CTL	(A)	A	P402-A
" "	(B)	B	P402-B
" "	(C)	C	P402-C
" "	(D)	D	P402-D
" "	(E)	E	P402-E
" "	(F)	F	P402-F
FILL CTL	(A)	H	P402-H
" "	(B)	J	P402-J
" "	(C)	K	P402-K
PULSE CTL	(A)	L	P402-L
" "	(B)	M	P402-M
" "	(C)	N	P402-N
BI-PHASE CTL	(A)	P	P402-P
" "	(B)	R	P402-R
" "	(C)	S	P402-S
VCO (4) SLCT		T	P402-T
NOISE/FILL CTL RTN		U	P402-U
PULSE, BI-PHASE, VCO SLCT RTN		36	P402-V

PART NUMBER	SIZE	WEST ASSEMBLY	QTY
SURFACE TREATMENT (SPPORS ABOVE)			

OL(6942A)
MODEL 14703A
P8

CONTROL (RF CHNL 4)
MS3116F-14-195
P402

A	P402-A
B	P402-B
C	P402-C
D	P402-D
E	P402-E
F	P402-F
H	P402-H
J	P402-J
K	P402-K
L	P402-L
M	P402-M
N	P402-N
P	P402-P
R	P402-R
S	P402-S
T	P402-T
U	P402-U
V	P402-V
36	

P8-A	A
P8-B	B
P8-C	C
P8-D	D
P8-E	E
P8-F	F
P8-H	H
P8-J	J
P8-K	K
P8-L	L
P8-M	M
P8-N	N
P8-P	P
P8-R	R
P8-S	S
P8-T	T
P8-U	U
P8-36	V
	G

NOISE CTL (A)
" " (B)
" " (C)
" " (D)
" " (E)
" " (F)
FILL CTL (A)
" " (B)
" " (C)
PULSE CTL (A)
" " (B)
" " (C)
BI-PHASE CTL (A)
" " (B)
" " (C)
VCO (4) SLCT
NOISE/FILL CTL RTN
PULSE, BI-PHASE, VCO SLCT RTN

REVISIONS				
ISSUE	OF	DATE	DESCRIPTION	APPROVED & DATE

DRAWN BY	ITEM NO.	UNL. CODE	PART OR IDENTIFYING NUMBER	CHECK ITEM OR CODE	NOMENCLATURE OR DESCRIPTION	STOCK CODE	MATERIAL AND/OR MATERIAL SPECIFICATION	TYPE CODE	ISSUE KEY
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UNLESS OTHERWISE SPECIFIED		REORDER 8/81		THE JOHNS HOPKINS UNIVERSITY APPLIED PHYSICS LABORATORY JOHNS HOPKINS ROAD LAUREL, MD 20606	
DIMENSIONS ARE IN INCHES TOLERANCES ON: XX ± .05 XXX ± .010 ANGULAR ± 1/2°		DATE		WIRING DIAGRAM, W7 MMG ECM SIMULATOR	
MATERIAL & TOL PER USAS 7545		DATE		CODE IDENT NO	
BREAK SHARP EDGES. REMOVE ALL BURRS		DATE		88898 C SK-A-7702-7	
WEIGHT		DATE		DO NOT SCALE PRINT	

Figure P-8 — Wiring diagram, W-7.

942A)
14703A

CONTROL (RF CHNL 5)
MS3116F-14-195
P502

P502-A

P502-A
P502-B
P502-C
P502-D
P502-E
P502-F
P502-H
P502-J
P502-K
P502-L
P502-M
P502-N
P502-P
P502-R
P502-S
P502-T
P502-U
P502-V

P9-A	A	NOISE CTL (A)
P9-B	B	" " (B)
P9-C	C	" " (C)
P9-D	D	" " (D)
P9-E	E	" " (E)
P9-F	F	" " (F)
P9-H	H	FILL CTL (A)
P9-J	J	" " (B)
P9-K	K	" " (C)
P9-L	L	PULSE CTL (A)
P9-M	M	" " (B)
P9-N	N	" " (C)
P9-P	P	BI-PHASE CTL (A)
P9-R	R	" " (B)
P9-S	S	" " (C)
P9-T	T	VCO (S) SLCT
P9-U	U	NOISE/FILL CTL RTN
P9-36	V	PULSE, BI-PHASE, VCO SLCT RTN
	G	

DATE	ITEM NO.	QTY	PART OR IDENTIFYING NUMBER	EXCISE SYMBOL OR MARK	NOMENCLATURE OR DESCRIPTION	STOCK CODE	MATERIAL AND/OR MATERIAL SPECIFICATION	QTY CODE	ISSUE NO.
LIST OF MATERIAL									
UNLESS OTHERWISE SPECIFIED					REEDER 8/61 DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS XX ± .05 XXX ± .010 ANGULAR ± 1/2° DIM. & TOL. PER ASME Y14.5 BREAK SHARP EDGES - REMOVE ALL BURRS				
THE JOHNS HOPKINS UNIVERSITY APPLIED PHYSICS LABORATORY JOHNS HOPKINS ROAD LAUREL, MD 20606					WIRING DIAGRAM, W8 MMG ECM SIMULATOR				
CODE IDENT NO. 88898 C SK-A-7702-8					ISSUE NO.				
DATE 8/61					DO NOT SCALE PRINT				

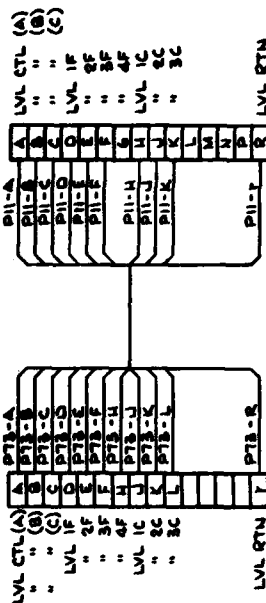
Figure P-9 — Wiring diagram, W-8.

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LAUREL, MARYLAND

CONTROL(6942A)
HP MODEL 14703A
PIO

NOISE	CTL	(A)	A	P602-A
"	"	(B)	B	P602-B
"	"	(C)	C	P602-C
"	"	(D)	D	P602-D
"	"	(E)	E	P602-E
"	"	(F)	F	P602-F
				P602-H
FILL	CTL	(A)	H	P602-H
"	"	(B)	J	P602-J
"	"	(C)	K	P602-K
			L	P602-L
PULSE	CTL	(A)	L	P602-L
"	"	(B)	M	P602-M
"	"	(C)	N	P602-N
			P	P602-P
BI-PHASE	CTL	(A)	P	P602-P
"	"	(B)	R	P602-R
"	"	(C)	S	P602-S
			T	P602-T
VCO (6) SLCT			T	P602-T
NOISE/FILL CTL RTN			r	P602-U
PULSE, BI-PHASE, VCO			36	P602-V
SLCT RTN				

[illegible]



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Figure P-12 — Wiring diagram, W-11.

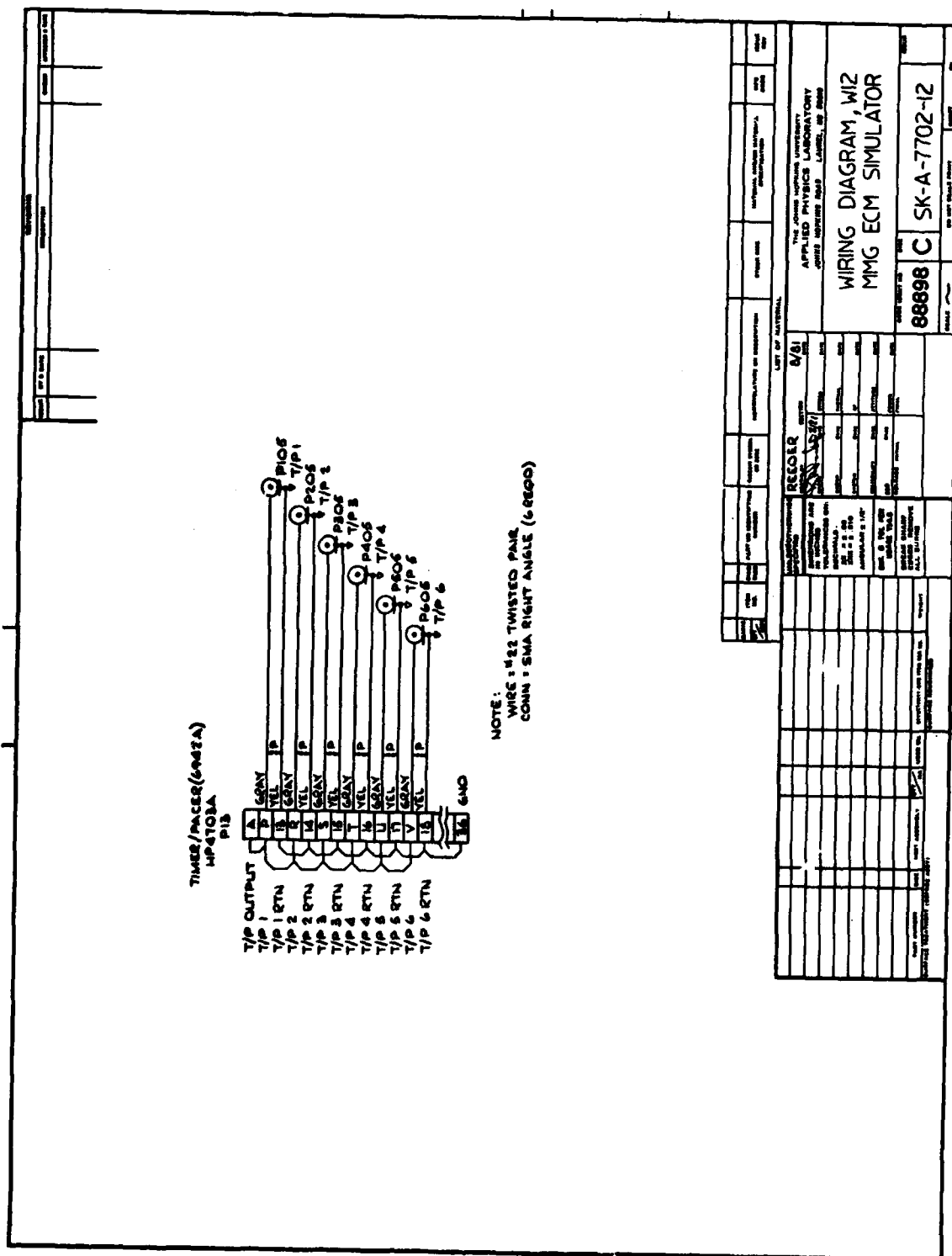


Figure P-13 — Wiring diagram, W-12.

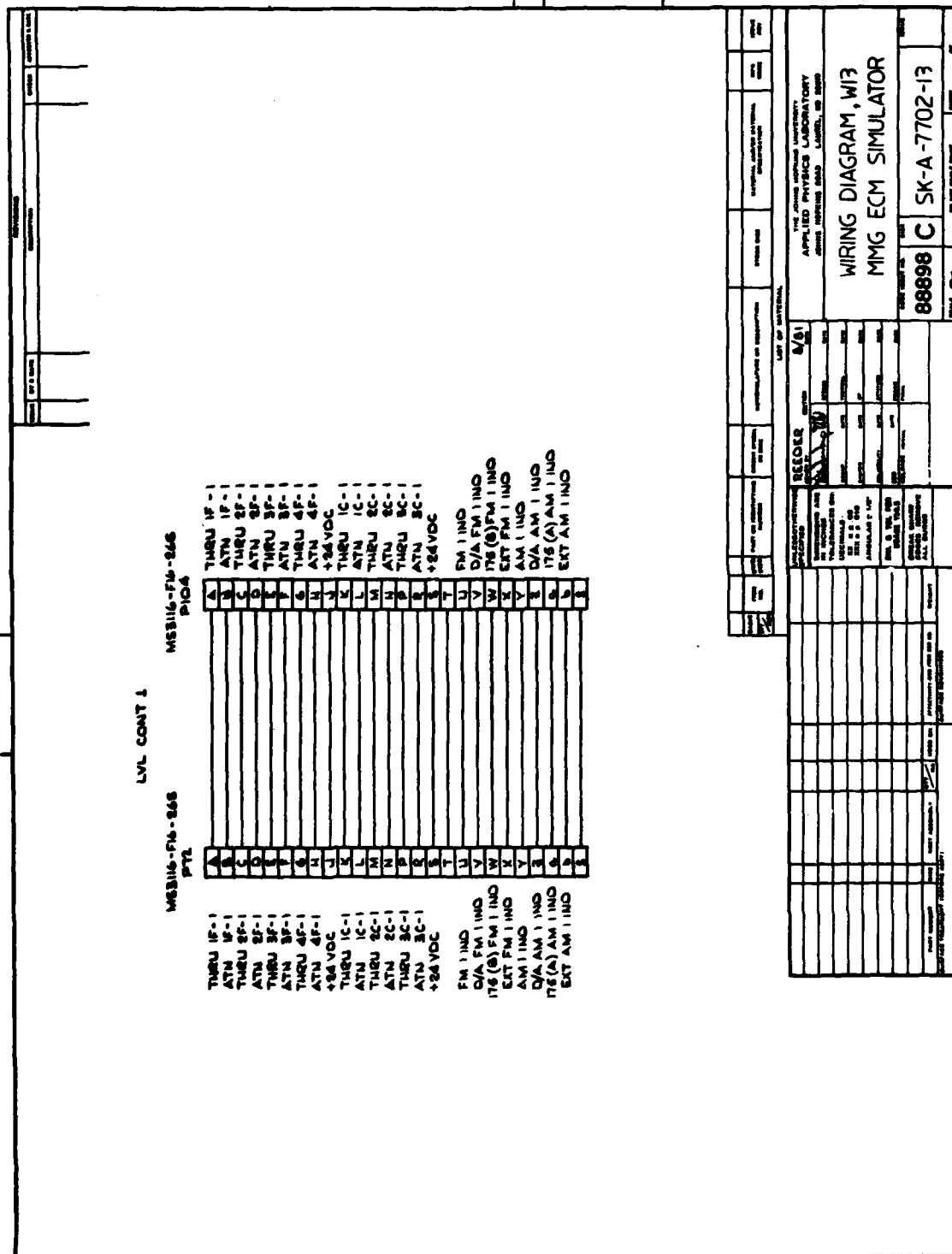


Figure P-14 -- Wiring diagram, W-13.

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LAUREL, MARYLAND

MS3116-F16-26S

P71

THRU 1F-2	A
ATN 1F-2	B
THRU 2F-2	C
ATN 2F-2	D
THRU 3F-2	E
ATN 3F-2	F
THRU 4F-2	G
ATN 4F-2	H
+24 VDC	J
THRU 1C-2	K
ATN 1C-2	L
THRU 2C-2	M
ATN 2C-2	N
THRU 3C-2	P
ATN 3C-2	R
+24 VDC	S
FM 2 INO	T
D/A FM 2 INO	U
175 (B) FM 2 INO	V
EXT FM 2 INO	W
AM 2 INO	X
D/A AM 2 INO	Y
175 (A) AM 2 INO	Z
EXT AM 2 INO	a
	b
	c

[illegible]

LVL CONT 2

MS3116-F16-265

MS3116-F16-265

P71

P204

2	A		A	THRU 1F-2
2	B		B	ATN 1F-2
2	C		C	THRU 2F-2
2	D		D	ATN 2F-2
2	E		E	THRU 3F-2
2	F		F	ATN 3F-2
2	G		G	THRU 4F-2
2	H		H	ATN 4F-2
2	J		J	+24VDC
2	K		K	THRU 1C-2
2	L		L	ATN 1C-2
2	M		M	THRU 2C-2
2	N		N	ATN 2C-2
2	P		P	THRU 3C-2
2	R		R	ATN 3C-2
2	S		S	+24VDC
2	T		T	
2	U		U	FM 2 IND
2 IND	V		V	D/A FM 2 IND
2 IND	W		W	175 (B) FM 2 IND
2 IND	X		X	EXT FM 2 IND
2	Y		Y	AM 2 IND
2 IND	Z		Z	D/A AM 2 IND
2 IND	a		a	175 (A) AM 2 IND
2 IND	b		b	EXT AM 2 IND
2	c		c	

BASIC	ITEM	QTY	UNIT	PART OR IDENTIFYING	CIRCUIT SYMBOL	NONEXCLATURE OR DESCRIPTION	STOCK SIZE	MATERIAL AND/OR MATERIAL	MFG	ISSUE
NO.	NO.		SIZE	NUMBER	OR CODE			SPECIFICATION	CODE	REV
LIST OF MATERIAL										
UNLESS OTHERWISE SPECIFIED				DRAWN BY		SECTION		DATE		
DIMENSIONS ARE IN INCHES				REEDER		8/81				
TOLERANCES ON:				DATE		DATE				
DECIMALS:				DATE		DATE				
XX ± .03				DATE		DATE				
XXX ± .010				DATE		DATE				
ANGULAR ± 1/2°				DATE		DATE				
GRL. & TOL PER				DATE		DATE				
USASI Y24.5				DATE		DATE				
BREAK SHARP				DATE		DATE				
EDGES - REMOVE				DATE		DATE				
ALL BURRS				DATE		DATE				
SURFACE FINISHES				DATE		DATE				
EFFECTIVITY AND ITEM NO.				DATE		DATE				
WEIGHT				DATE		DATE				
MFG CODE				DATE		DATE				
ISSUE REV				DATE		DATE				
THE JOHNS HOPKINS UNIVERSITY				DATE		DATE				
APPLIED PHYSICS LABORATORY				DATE		DATE				
JOHNS HOPKINS ROAD LAUREL, MD 20610				DATE		DATE				
WIRING DIAGRAM, W14				DATE		DATE				
MMG ECM SIMULATOR				DATE		DATE				
CODE IDENT NO				DATE		DATE				
88898				DATE		DATE				
SIZE				DATE		DATE				
C				DATE		DATE				
SK-A-7702-14				DATE		DATE				
SCALE				DATE		DATE				
DO NOT SCALE PRINT				DATE		DATE				
SHEET				DATE		DATE				
OF				DATE		DATE				

Figure P-15 — Wiring diagram, W-14.

				UNLESS OTHERWISE SPECIFIED				REORDER DATE <u>8/8/79</u> BY <u>5919</u>				THE JOHNS HOPKINS UNIVERSITY APPLIED PHYSICS LABORATORY JOHNS HOPKINS ROAD LAUREL, MD 20606			
				DIMENSIONS ARE IN INCHES TOLERANCES ON: DIMENSIONS: $\pm .005$ HOLE: $\pm .010$ ANGULAR: $\pm 1/2^\circ$ SURF. & TOL. PER ASME Y14.5				DATE <u>8/8/79</u> BY <u>5919</u> CHECKED <u>DATE</u> BY <u>DATE</u> APPROVED <u>DATE</u> BY <u>DATE</u> RELEASE: <u>DATE</u> BY <u>DATE</u>				WIRING DIAGRAM, W15 MMG ECM SIMULATOR			
NEXT ASSEMBLY <u>DATE</u> USED ON <u>DATE</u> APPROVED FOR USE ON <u>DATE</u> BY <u>DATE</u>				BREAK DOWN EDGES - REMOVE ALL BURRS				CODE IDENT. NO. 88898				C SK-A-7702-15			
SCALE <u>DATE</u>				NO NET SCALE POINT				CHECK <u>DATE</u>				BY <u>DATE</u>			

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MS3116-F16-26S
P69

THRU 1F-4	A
ATN 1F-4	B
THRU 2F-4	C
ATN 2F-4	D
THRU 3F-4	E
ATN 3F-4	F
THRU 4F-4	G
ATN 4F-4	H
+24 VDC	J
THRU 1C-4	K
ATN 1C-4	L
THRU 2C-4	M
ATN 2C-4	N
THRU 3C-4	P
ATN 3C-4	R
+24 VDC	S
FM 4 INO	T
O/A FM 4 INO	U
175 (B) FM 4 INO	V
EXT FM 4 INO	W
AM 4 INO	X
O/A AM 4 INO	Y
176 (A) AM 4 INO	Z
EXT AM 4 INO	a
	b
	c

[illegible]

LVL CONT 4

REVISIONS			
NO.	BY & DATE	DESCRIPTION	APPROVED & DATE

3116-F16-265
P69

MS3116-F16-265
P404

A	THRU 1F-4
B	ATN 1F-4
C	THRU 2F-4
D	ATN 2F-4
E	THRU 3F-4
F	ATN 3F-4
G	THRU 4F-4
H	ATN 4F-4
J	+24VDC
K	THRU 1C-4
L	ATN 1C-4
M	THRU 2C-4
N	ATN 2C-4
P	THRU 3C-4
R	ATN 3C-4
S	+24VDC
T	
U	FM 4 IND
V	O/A FM 4 IND
W	175(B) FM 4 IND
X	EXT FM 4 IND
Y	AM 4 IND
Z	O/A AM 4 IND
a	175(A) AM 4 IND
b	EXT AM 4 IND
s	

RANK	ITEM NO.	QTY	PART OR IDENTIFYING NUMBER	CHECK SYMBOL OR QTY	DESCRIPTION OR DESCRIPTION	STOCK SIZE	MATERIAL AND/OR MATERIAL SPECIFICATION	NPS CODE	ISSUE REV
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LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED		REORDER		8/81		THE JOHNS HOPKINS UNIVERSITY APPLIED PHYSICS LABORATORY JOHNS HOPKINS ROAD LAUREL, MD 20800	
DIMENSIONS ARE IN INCHES		8/81		8/81		WIRING DIAGRAM, W16	
TOLERANCES ON:		8/81		8/81		MMG ECM SIMULATOR	
DECIMALS:		8/81		8/81		CODE IDENT NO	
XX ± .00		8/81		8/81		88898	
XXX ± .010		8/81		8/81		C	
ANGULAR ± 1/2°		8/81		8/81		SK-A-7702-16	
GRL & TOL FOR		8/81		8/81		ISSUE	
MFGS TOL		8/81		8/81		88898	
BREAK SHARP		8/81		8/81		C	
CORNER - REMOVE		8/81		8/81		SK-A-7702-16	
ALL SURF		8/81		8/81		ISSUE	
		8/81		8/81		88898	
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		8/81		8/81		ISSUE	
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		8/81		8/81		ISSUE	
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		8/81					

THE JOHNS HOPKINS UNIVERSITY
APPLIED PHYSICS LABORATORY
LAUREL, MARYLAND

LVL

MS3116-F16-265
P68

THRU 1F-5
ATN 1F-5
THRU 2F-5
ATN 2F-5
THRU 3F-5
ATN 3F-5
THRU 4F-5
ATN 4F-5
+24 VDC
THRU 1C-5
ATN 1C-5
THRU 2C-5
ATN 2C-5
THRU 3C-5
ATN 3C-5
+24 VDC

FM 5 INO
D/A FM 5 INO
175 (B) FM 5 INO
EXT FM 5 INO
AM 5 INO
D/A AM 5 INO
175 (A) AM 5 INO
EXT AM 5 INO

A	
B	
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PART NUMBER	QTY.	PART ASSEMBLY	DFT %
SUBMIT MATERIALS REPORT AND:			

LVL CONT 5

-F16-268

MS3116-F16-268
PS04

REVISIONS			
NO.	DATE	DESCRIPTION	APPROVED & DATE

	A	THRU 1F-5
	B	ATN 1F-5
	C	THRU 2F-5
	D	ATN 2F-5
	E	THRU 3F-5
	F	ATN 3F-5
	G	THRU 4F-5
	H	ATN 4F-5
	J	+24VDC
	K	THRU 1C-5
	L	ATN 1C-5
	M	THRU 2C-5
	N	ATN 2C-5
	P	THRU 3C-5
	R	ATN 3C-5
	S	+24VDC
	T	
	U	FM 5 IND
	V	O/A FM 5 IND
	W	175 (B) FM 5 IND
	X	EXT FM 5 IND
	Y	AM 5 IND
	Z	O/A AM 5 IND
	a	175 (A) AM 5 IND
	b	EXT AM 5 IND
	c	

ITEM NO.	QTY	PART NO IDENTIFYING NUMBER	UNIT QTY	DESCRIPTION OR IDENTIFICATION	STOCK NO.	MATERIAL AND/OR MATERIAL SPECIFICATION	QTY	ISSUE
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LIST OF MATERIAL

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DIMENSIONS ARE IN INCHES		TOLERANCES ON:		FRACTIONS		DECIMALS	
DECIMALS:		FRACTIONS:		FRACTIONS:		DECIMALS:	
BY ± 0.00		BY ± 0.010		BY ± 0.010		BY ± 0.010	
ANGULAR ± 1/2°		ANGULAR ± 1/2°		ANGULAR ± 1/2°		ANGULAR ± 1/2°	
MIL. & VOL. PER		MIL. & VOL. PER		MIL. & VOL. PER		MIL. & VOL. PER	
GRADE 101.0		GRADE 101.0		GRADE 101.0		GRADE 101.0	
BREAD BOARD		BREAD BOARD		BREAD BOARD		BREAD BOARD	
CIRCUITS - REMOVE		CIRCUITS - REMOVE		CIRCUITS - REMOVE		CIRCUITS - REMOVE	
ALL SURF		ALL SURF		ALL SURF		ALL SURF	
REMARKS: INITIAL		REMARKS: INITIAL		REMARKS: INITIAL		REMARKS: INITIAL	
DATE		DATE		DATE		DATE	
SIGNATURE		SIGNATURE		SIGNATURE		SIGNATURE	
DATE		DATE		DATE		DATE	
88898		C		SK-A-7702-17		88898	
DO NOT SCALE PRINT		DO NOT SCALE PRINT		DO NOT SCALE PRINT		DO NOT SCALE PRINT	

Figure P-18 — Wiring diagram, W-17.

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APPLIED PHYSICS LABORATORY
LAUREL, MARYLAND

MS3116-F16-26S
P67

THRU 1F-6
 ATN 1F-6
 THRU 2F-6
 ATN 2F-6
 THRU 3F-6
 ATN 3F-6
 THRU 4F-6
 ATN 4F-6
 +24 VDC
 THRU 1C-6
 ATN 1C-6
 THRU 2C-6
 ATN 2C-6
 THRU 3C-6
 ATN 3C-6
 +24 VDC
 FM 6 INO
 D/A FM 6 INO
 175 (8) FM 6 INO
 EXT FM 6 INO
 AM 6 INO
 D/A AM 6 INO
 175 (A) AM 6 INO
 EXT AM 6 INO

A	
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N	
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R	
S	
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U	
V	
W	
X	
Y	
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a	
b	
c	

PART NUMBER	SERIAL	MOUNT ADDRESS/VOL.	DWG NO.

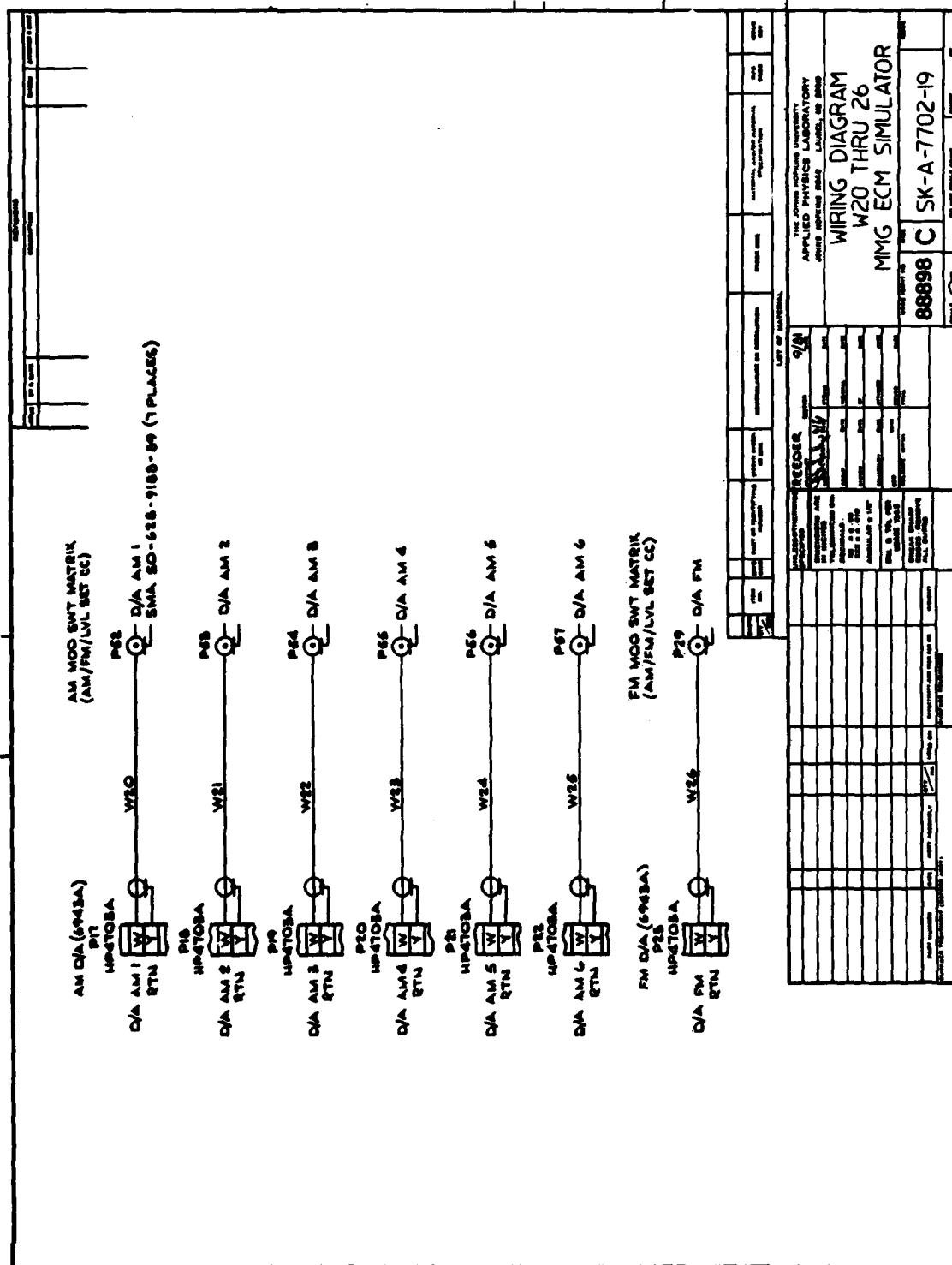


Figure P-20 — Wiring diagram, W-20 through W-26

APPENDIX Q

DRAWING LIST OF THE MMG LOW FREQUENCY ECM SIMULATOR

Figure	Drawing	Title	Figure	Drawing	Title
A-1	SK-A-7701	Block diagram of MMG low frequency ECM simulator	O-1	SK-A-7646	Power supply assembly, type I
B-6	SK-A-7601	RF assembly, type I wiring diagram	O-2	SK-A-7647	Power supply assembly, type II
B-7	SK-A-7616	RF assembly, type II wiring diagram	P-1	SK-A-7702	Cabling, inter-rack
C-2	SK-A-7578	Schematic, VCO driver type I	P-2	SK-A-7702-1	Wiring diagram, W-1
C-3	SK-A-7582	Schematic, VCO driver type II	P-3	SK-A-7702-2	Wiring diagram, W-2
D-1	SK-A-7650	Noise filters and fill oscillator	P-4	SK-A-7702-3	Wiring diagram, W-3
E-1	SK-A-7654	Fill oscillator attenuators	P-5	SK-A-7702-4	Wiring diagram, W-4
E-2	SK-A-7655	Noise attenuators	P-6	SK-A-7702-5	Wiring diagram, W-5
F-1	SK-A-7652	RF relay driver	P-7	SK-A-7702-6	Wiring diagram, W-6
G-1	SK-A-7651	Biphase modulator	P-8	SK-A-7702-7	Wiring diagram, W-7
H-1	SK-A-7653	Pulse modulation selector	P-9	SK-A-7702-8	Wiring diagram, W-8
I-1	SK-A-7703	AM modulation switch matrix	P-10	SK-A-7702-9	Wiring diagram, W-9
I-2	SK-A-7704	FM modulation switch matrix	P-11	SK-A-7702-10	Wiring diagram, W-10
J-1	SK-A-7705	Level-set attenuator driver	P-12	SK-A-7702-11	Wiring diagram, W-11
L-1	SK-A-7669	AM/FM level-set card cage wiring	P-13	SK-A-7702-12	Wiring diagram, W-12
M-1	SK-A-7749	Wiring front panel	P-14	SK-A-7702-13	Wiring diagram, W-13
N-1	SK-A-7748	Card cage wiring diagram	P-15	SK-A-7702-14	Wiring diagram, W-14
			P-16	SK-A-7702-15	Wiring diagram, W-15
			P-17	SK-A-7702-16	Wiring diagram, W-16
			P-18	SK-A-7702-17	Wiring diagram, W-17
			P-19	SK-A-7702-18	Wiring diagram, W-18
			P-20	SK-A-7702-19	Wiring diagram, W-20 through W-26

APPENDIX R

RF CHANNEL TESTER

A RF channel tester was developed that allows an operator to manually exercise all the control and modulation functions of one RF channel. Figure R-1 is a photograph of the tester.

The channel tester can select one of the two VCO modules, tune the VCO center frequency, control the noise video filter bandwidth, select the noise and fill attenuation values, select the form and source of the biphase and pulse modulation, and operate the level-set attenuator. These functions are controlled by the toggle switches on the tester's front panel.

The tester has internal oscillators to simulate both the auxiliary FM and AM inputs. The frequencies, amplitudes, waveshapes, and DC offset levels of these oscillators may be independently controlled.

The output of a free-running pulse generator is also available at the front panel as a modulation source.

Feedthrough connections to the timer/pacer, external, and Wavetek A and B inputs are provided to simplify the wiring when these sources are used to modulate the RF channel under test. These feedthrough connections also include test points to allow the operator to monitor the inputs from these modulation sources.

A cable harness connects all signals except power to the rear panel connectors of the RF channel under test. The operator may use this tester to examine all the operating modes of an RF channel for servicing or use a single RF channel in a manual mode for ECM testing.

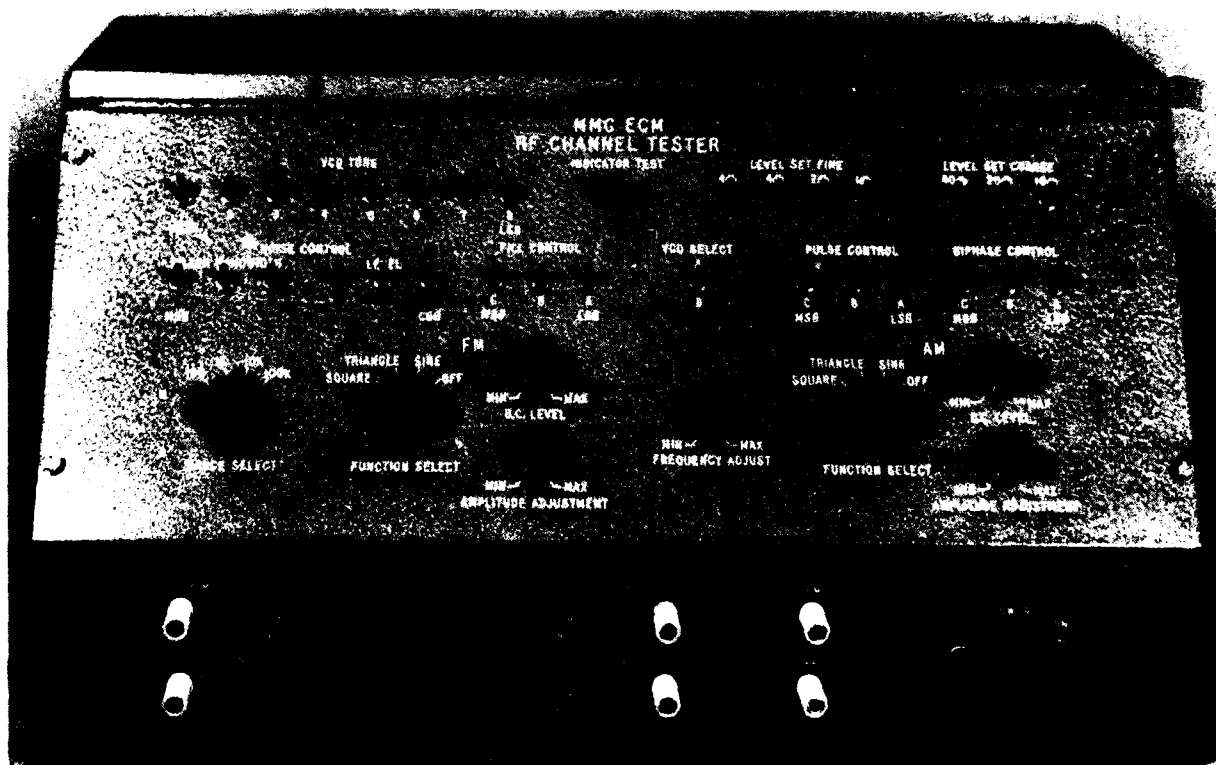


Figure R-1 — RF channel tester.

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		SEA-62	1
		SEA-62Q	1
		SEA-62R	1
		SEA-62R1	1
		SEA-62R5	1
		SEA-62R55	5
		SEA-62R57	1
		SEA-62R3	1
		SEA-62R31P	1
		PMS-400B	1
		PMS-400M	1
		Library	1
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		AIR-360	1
		AIR-360R	1
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		F-42	1
		F-46	1
		Library	1
Naval Weapons Center	China Lake, CA	3906	7
		3921	1
		39501	1
		Library	1
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